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File Name :

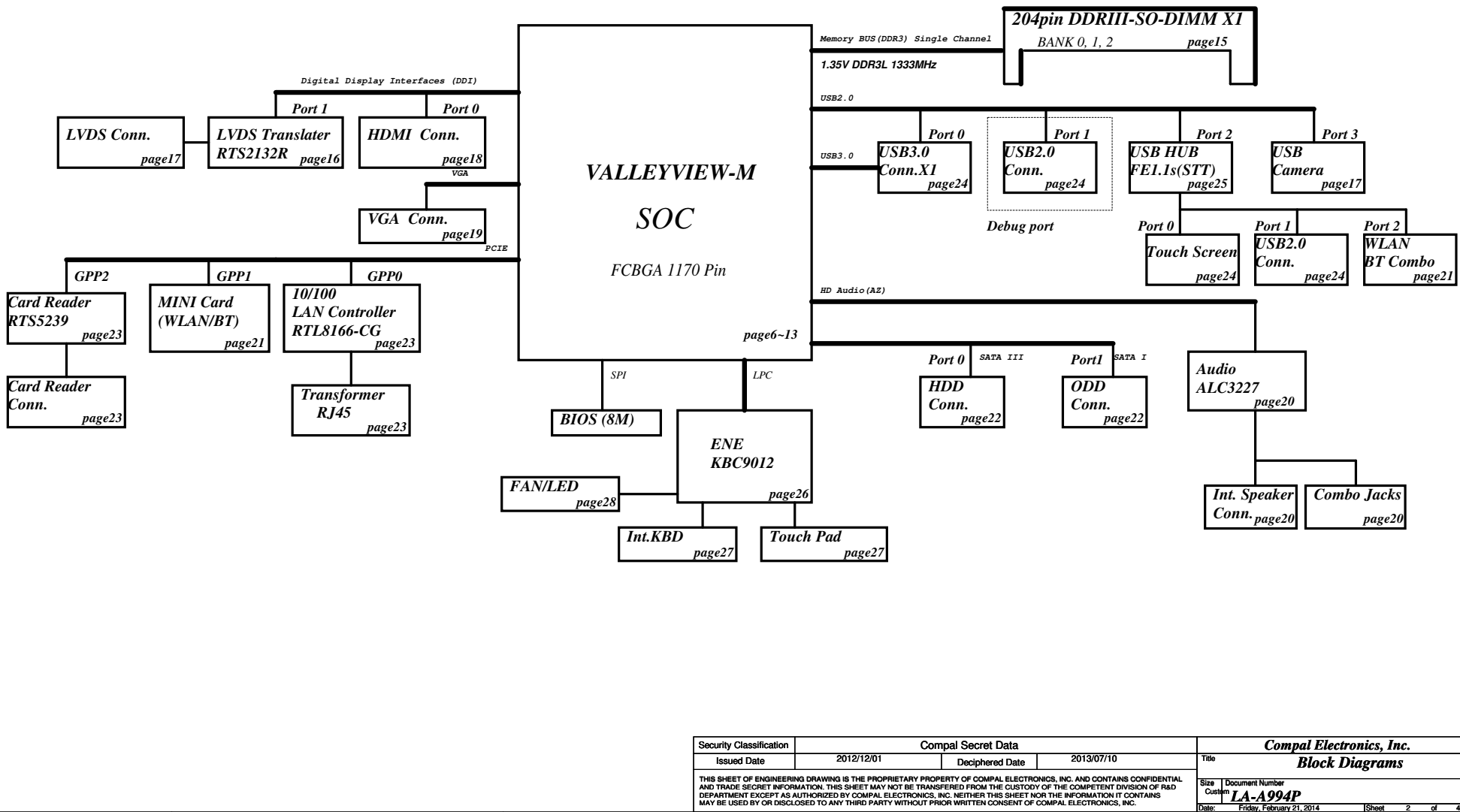
# Compal Confidential

## *ULC UMA M/B LA-A994P Schematics Document*

Intel Bay Trail M VC  
Project Code : ZSO50  
2014/02/05  
MV Rev. 1.0

DAX ZSO50 BayTrail-M	
Part Number	Description
DAZ14Z00200	PCB 14Z LA-A994P REV0 M/B 4

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title Cover Page	
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/12/01	Deciphered Date	2013/07/10	Title Block Diagrams	
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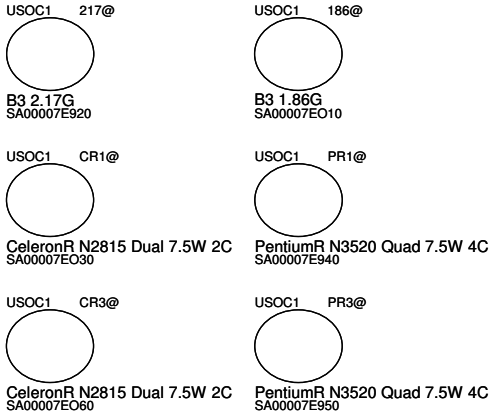
Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

BOARD ID Table

Board ID	PCB Revision
DB	0.1
SI	0.2
PV	0.3
MV	1.0

BOM Option Table	
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMI requirement	EMI@
EMI requirement unpop	@EMI@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
8161 LAN controller	8161@
8166 LAN controller	8166@
LVDS	LVDS@
LVDS LDO mode	LVDSLDO@
LVDS SWR mode	LVDSSWR@
Translator RTS2132S	2132S@
Translator RTS2132R	2132R@
Short Pad	RS@
Clean CMOS	CMOS@
Jump	JP@



EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

SOC SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X JDIMM1(SPD)

43 level BOM table

43 Level	Description	BOM Structure
4319P6BOL01	SMT MB AA231 V1UE3 HDMI	

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**LA-A994P**

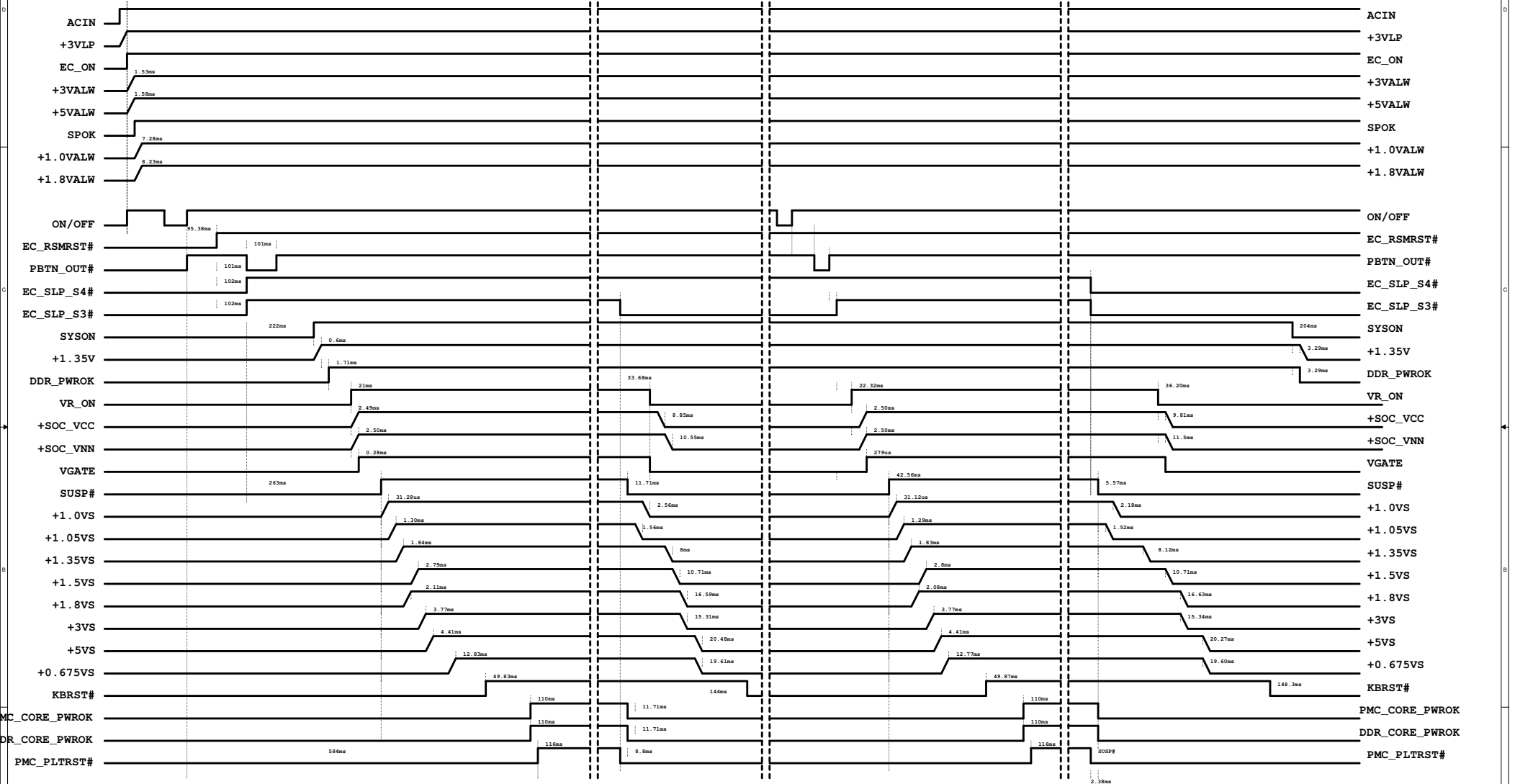
Rev  
0.1

G3-&gt;S0

S0-&gt;S3

S3-&gt;S0

S0-&gt;S5

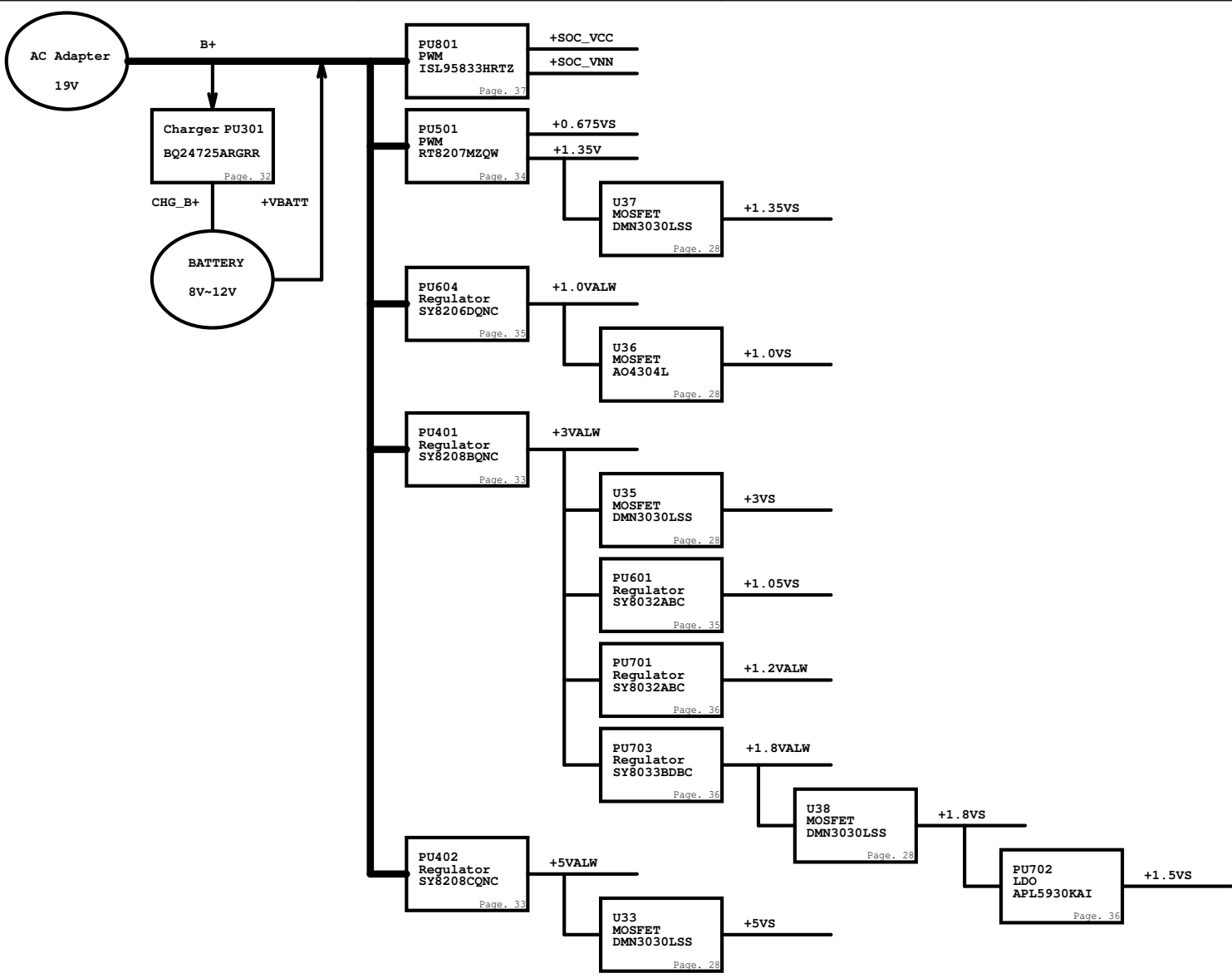


## NOTE:

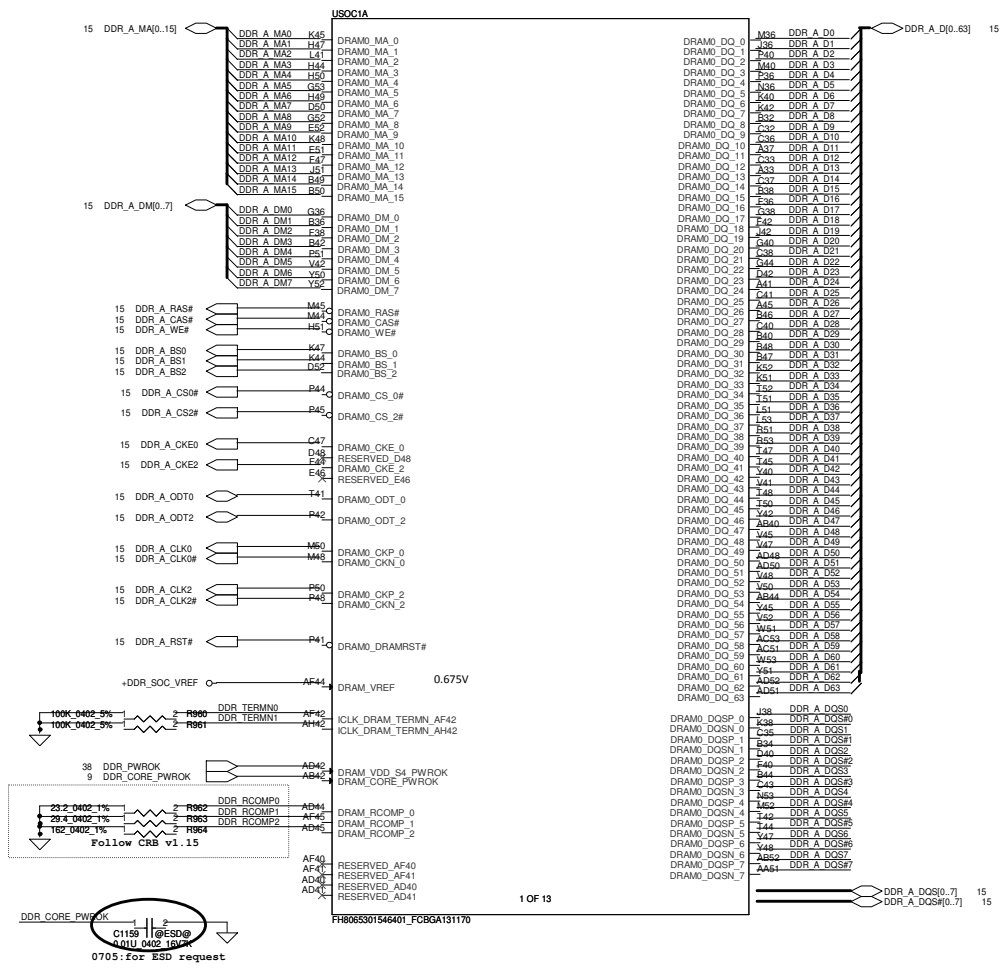
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

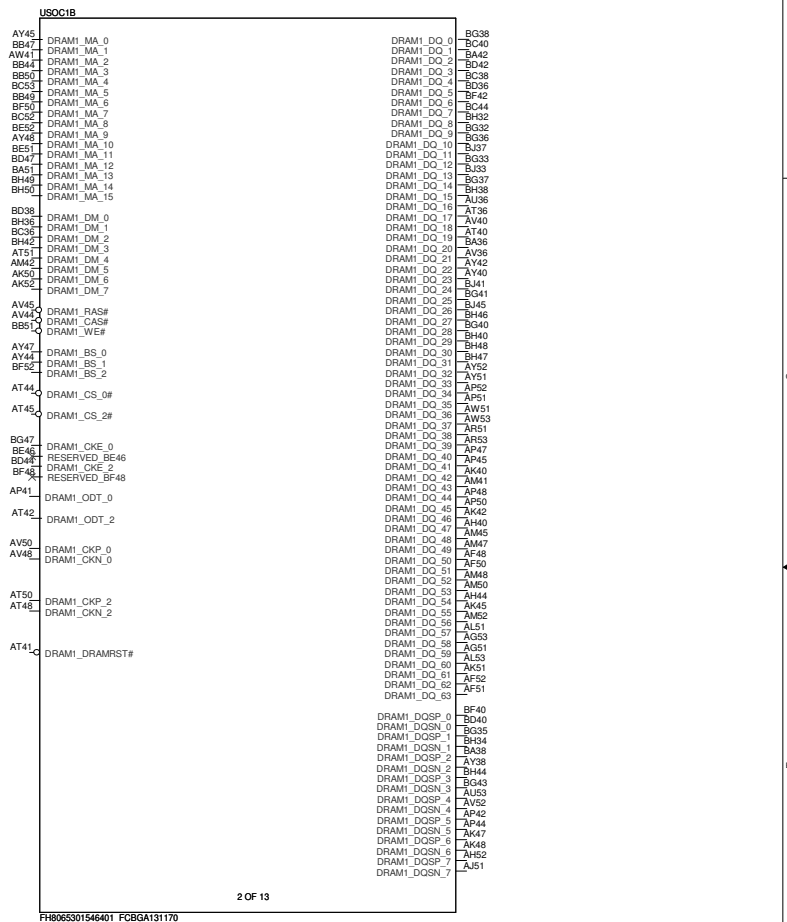
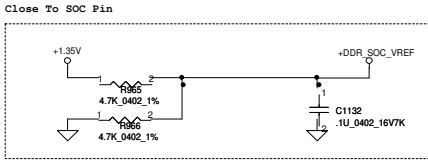
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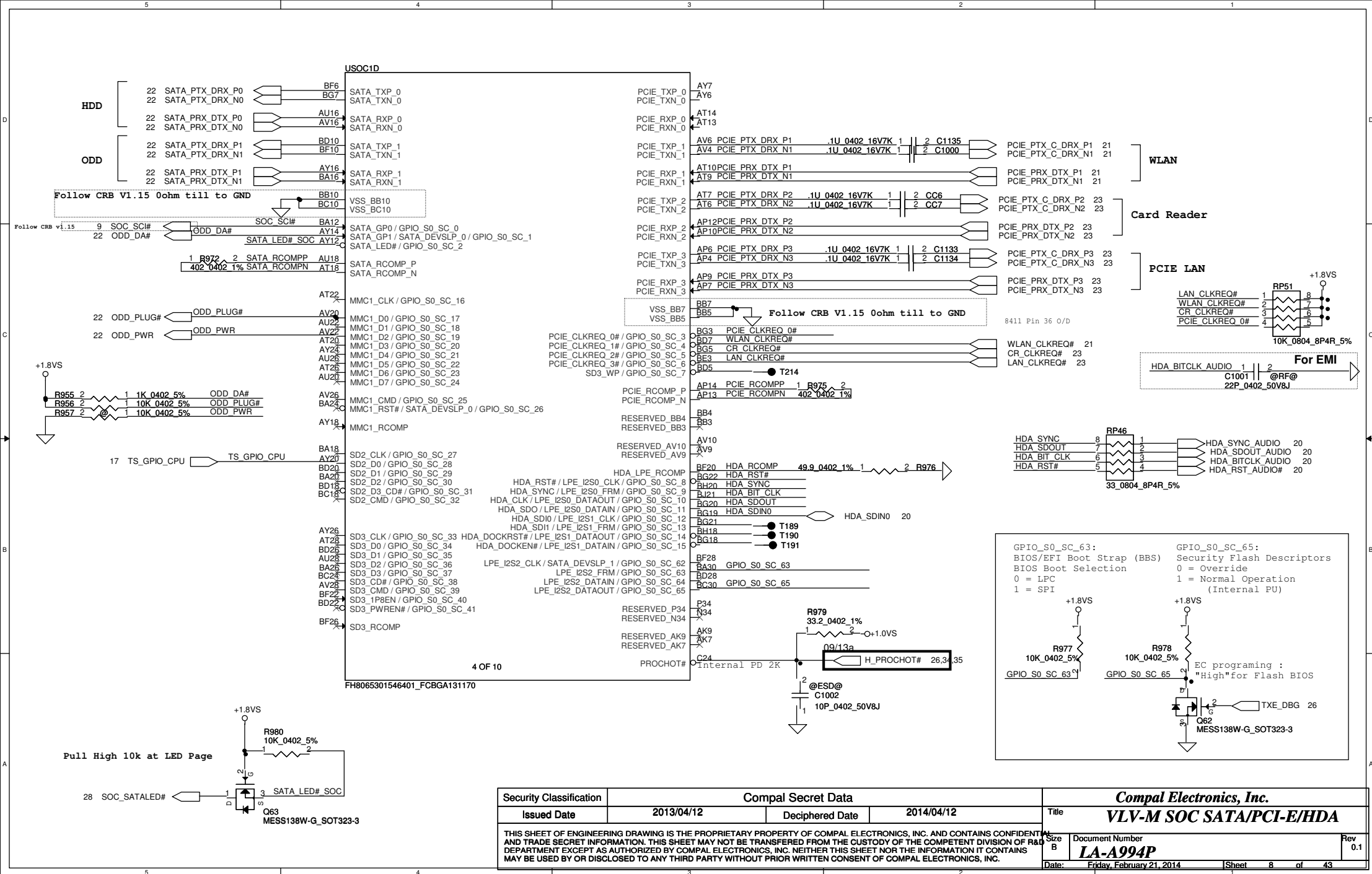


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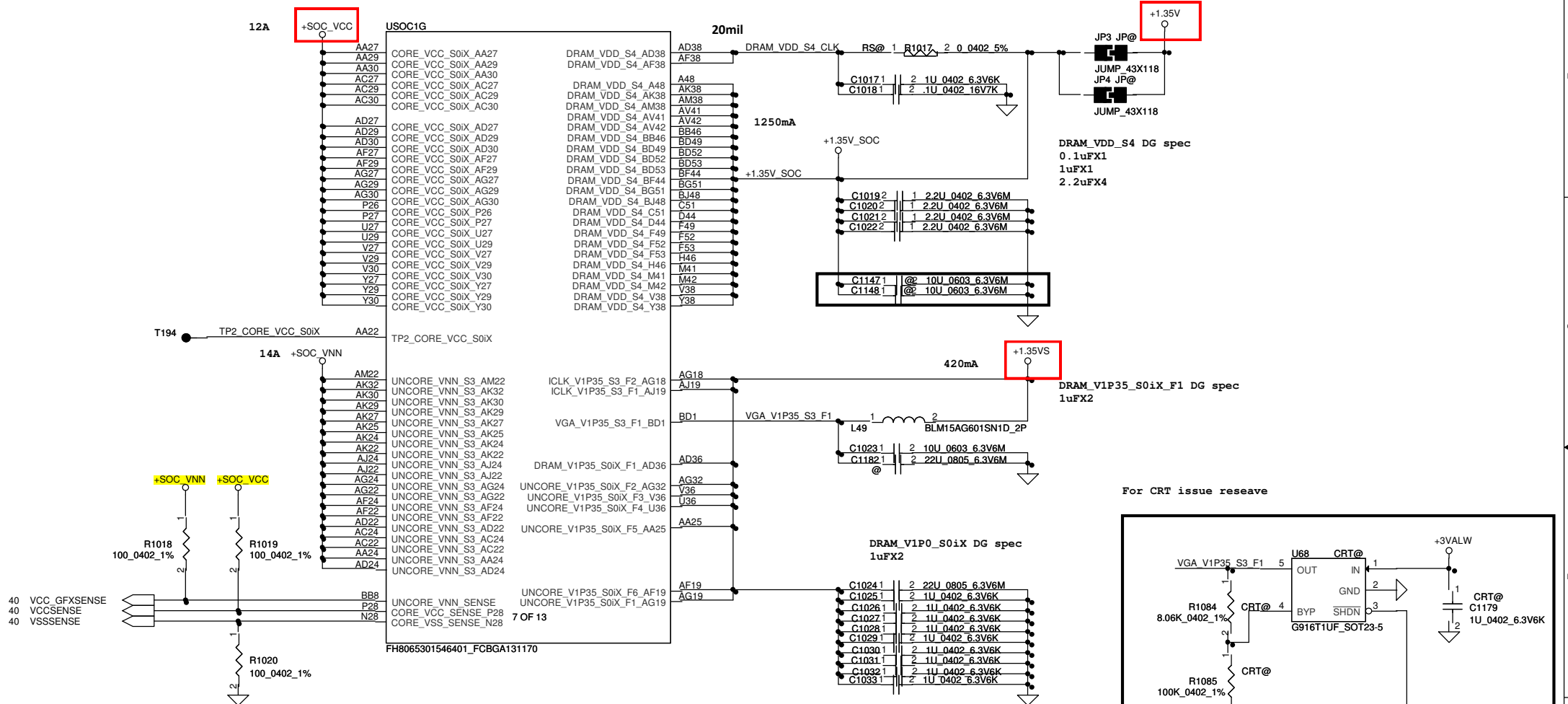




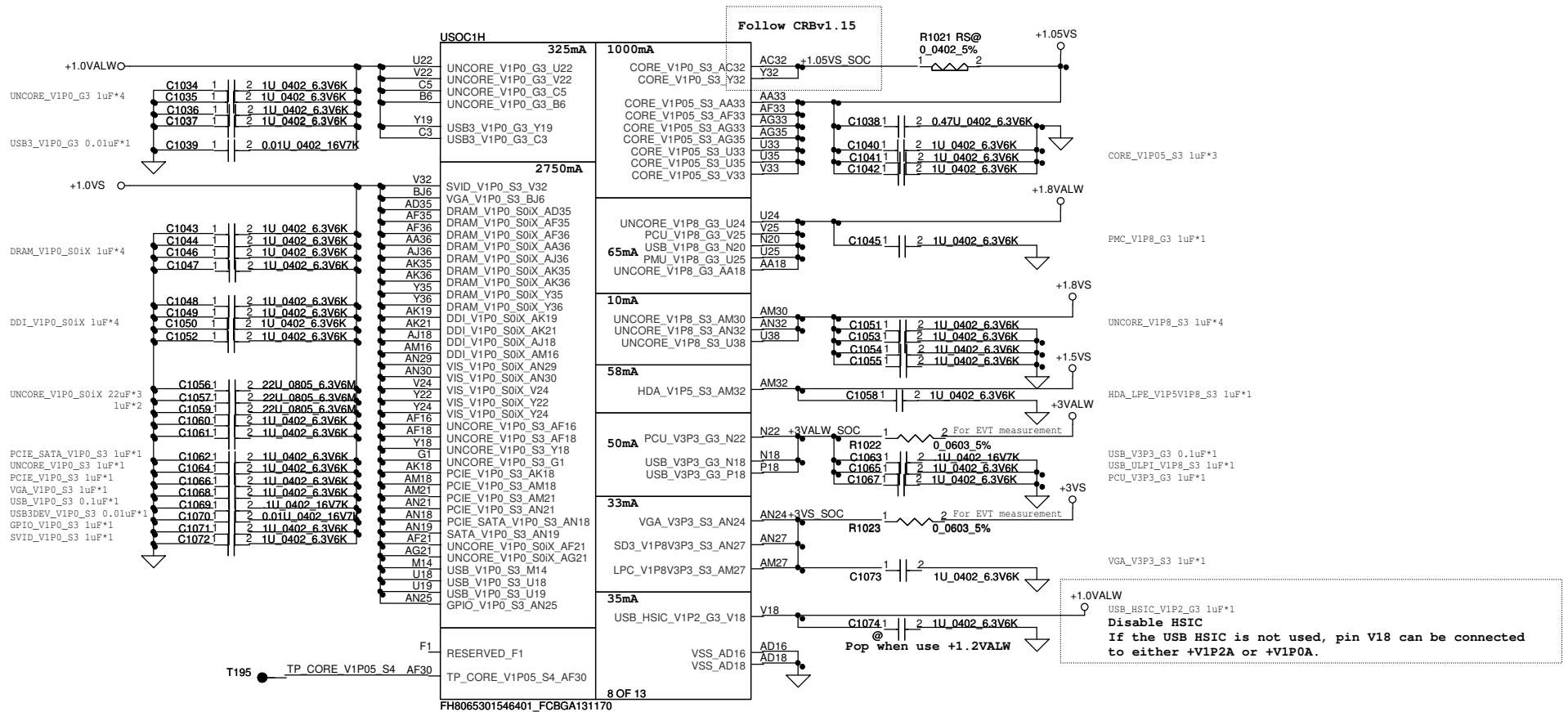




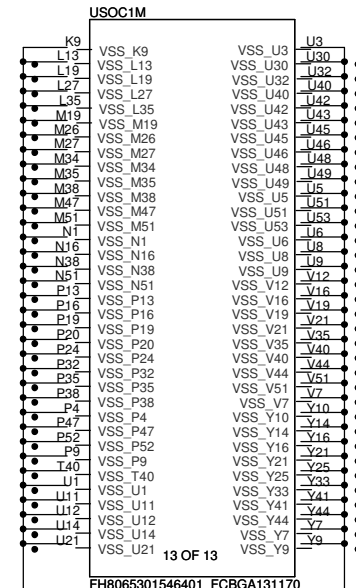
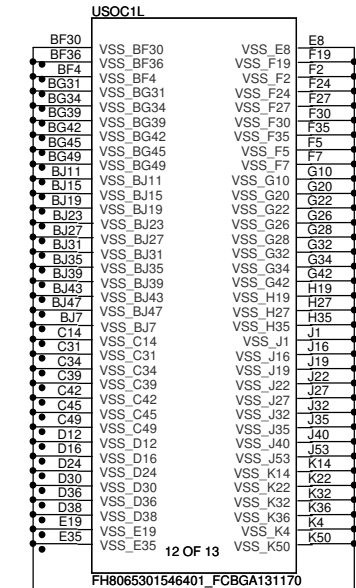
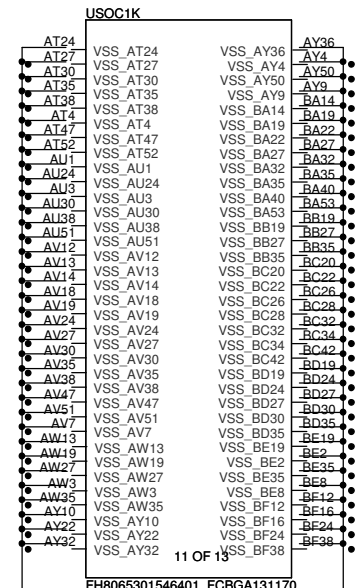
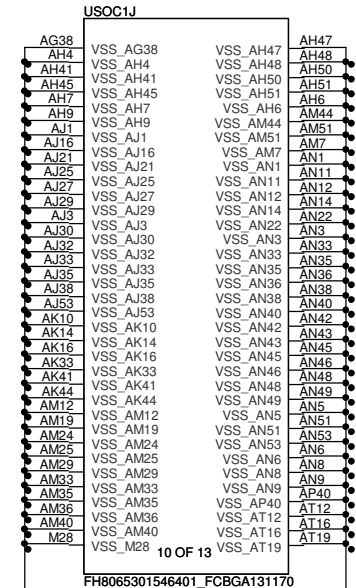
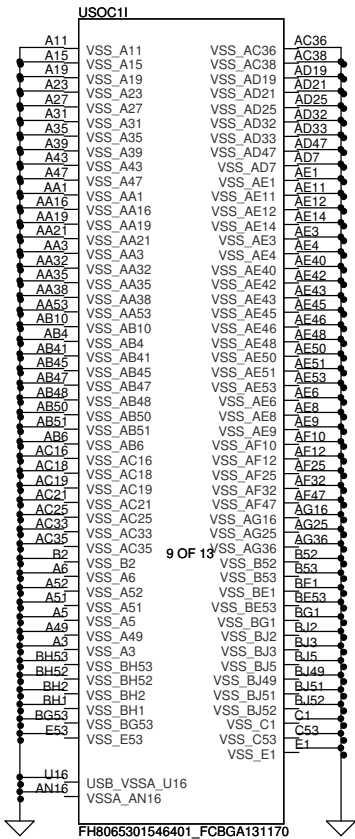




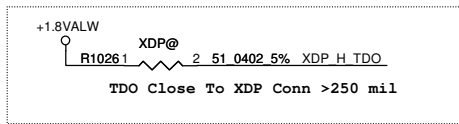
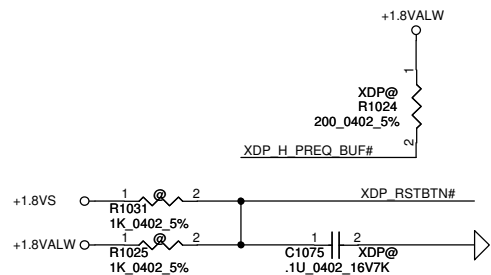
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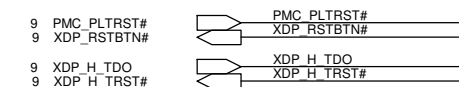
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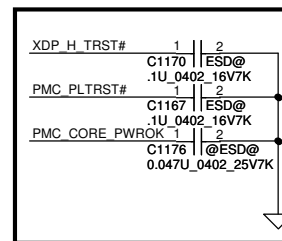
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## XDP-SFF-26Pin

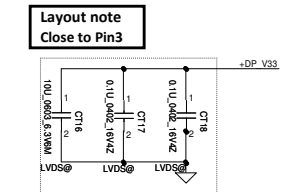
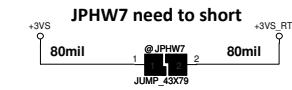


0927:for ESD request



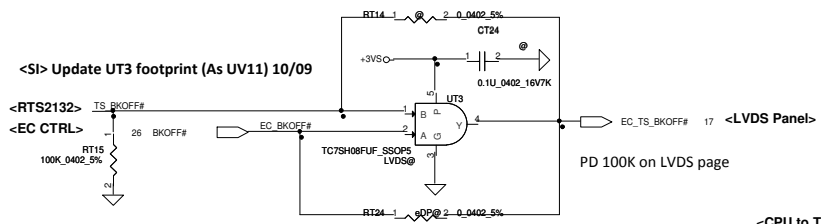
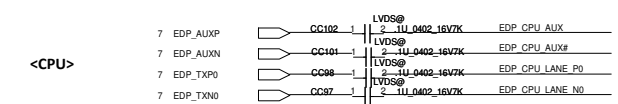
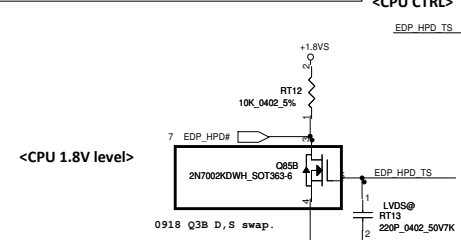
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	VLV-M SOC Debug
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SWR / LDO Mode select		
	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

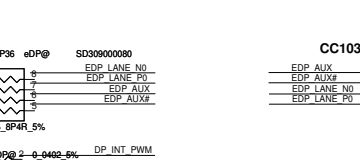
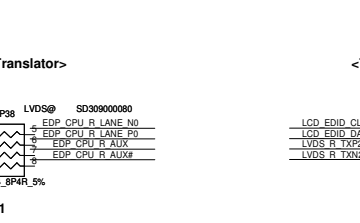
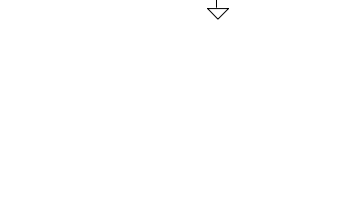
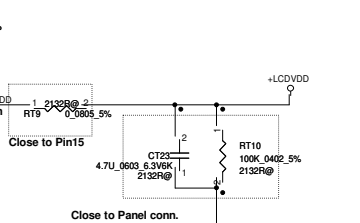
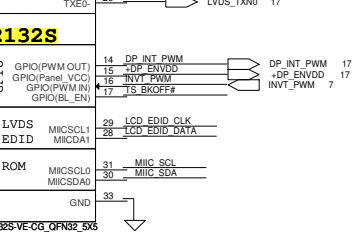
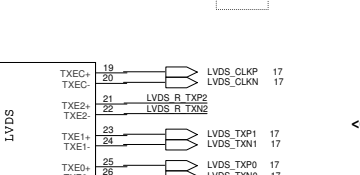
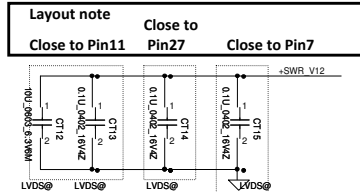
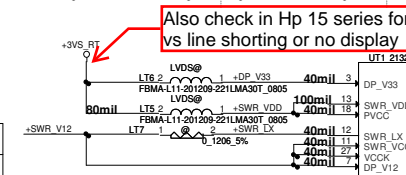
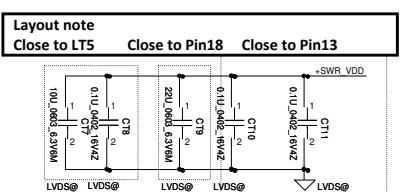
\* If use 2132R, please select LDO mode as default.



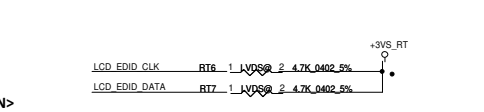
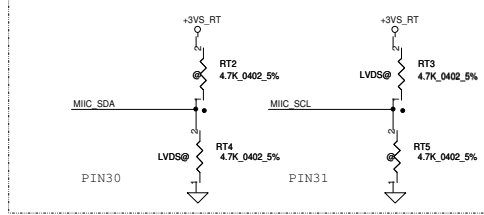
131111 add RT15 for power sequence

**<LVDS panel> ==>**

**<eDP panel> ==>**



**\*ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.**  
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.  
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.  
( \*Default mode )



PIN15	
2132S	TL_ENVDD
2132R	+LCD_VDD *

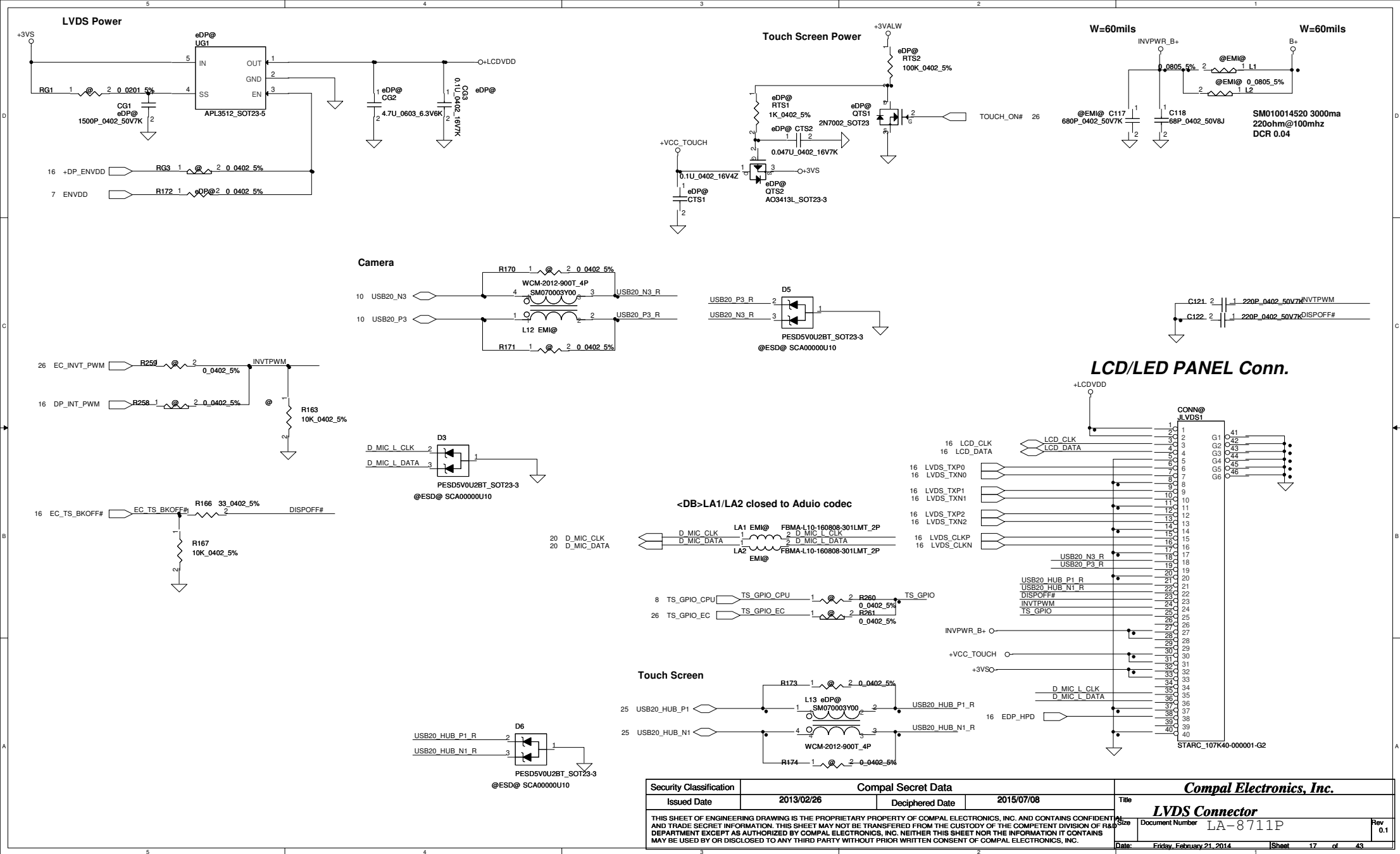
\* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16		Accept voltage input (high level)
2132S		3.3V
2132R		1.5~3.3V

\* Version R has internal level shifter, remove level shifter circuit on AMD platform

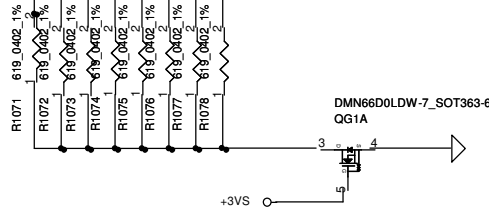
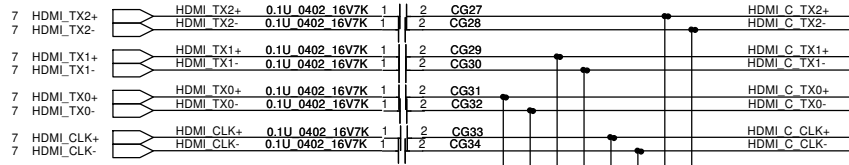
Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter



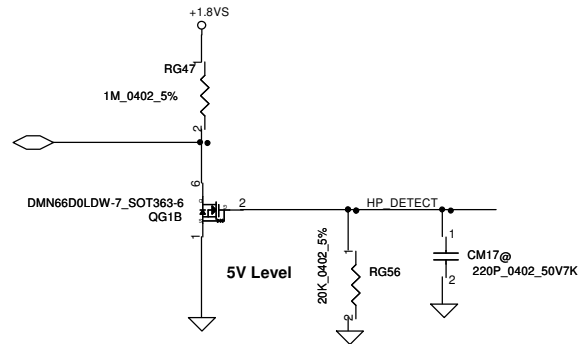


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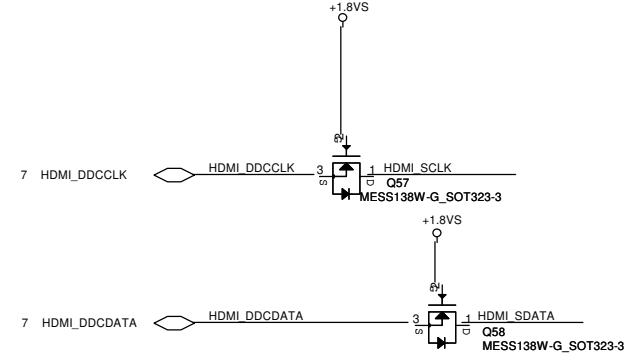
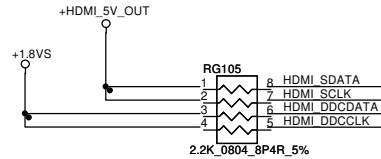
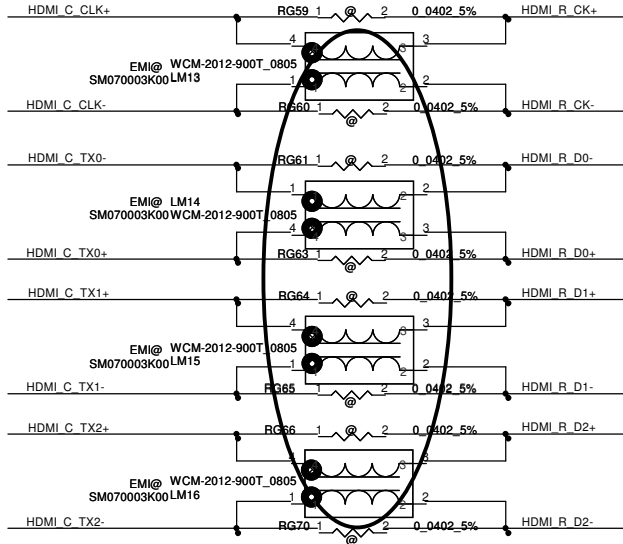
D2  
D1  
D0  
CLK



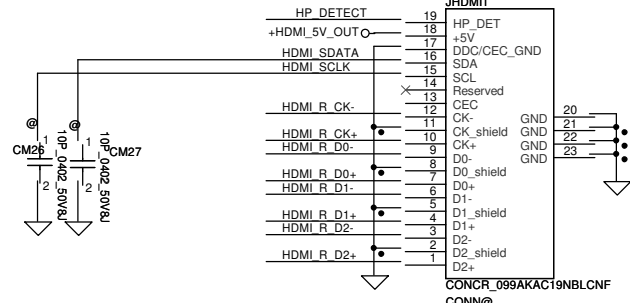
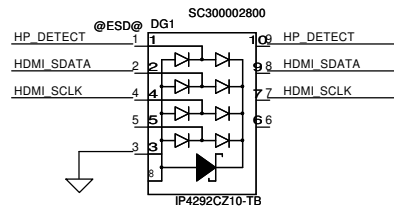
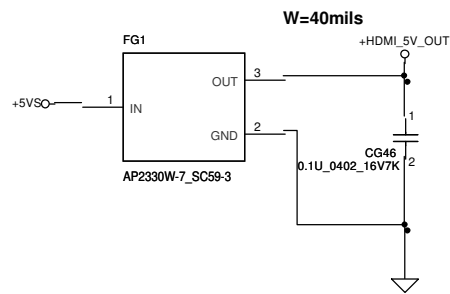
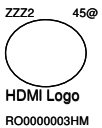
7 HDMI\_HP#



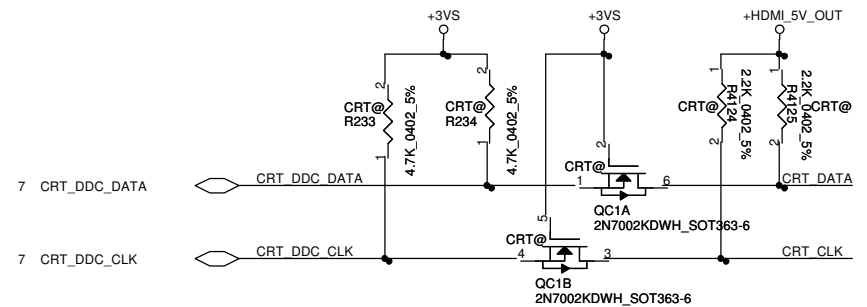
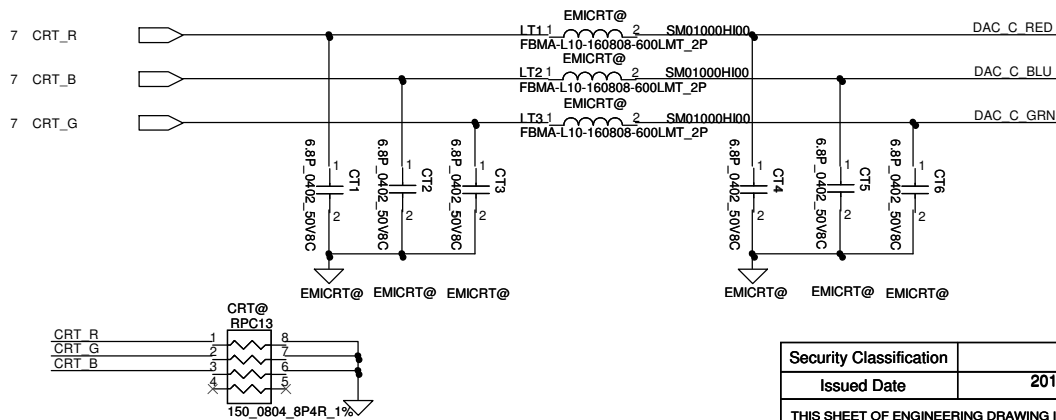
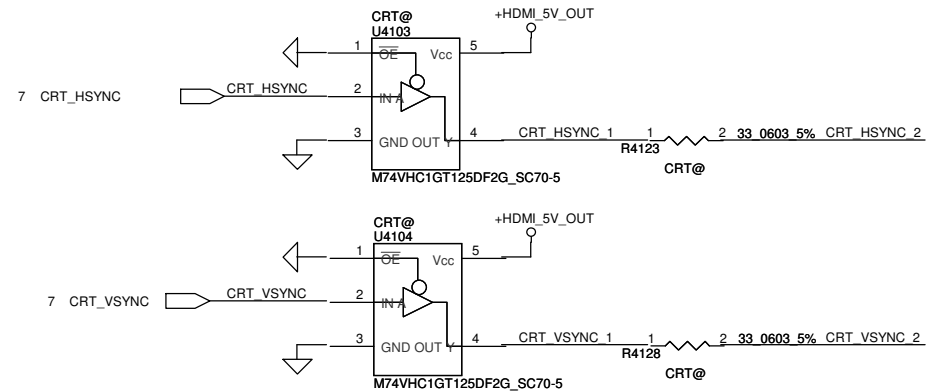
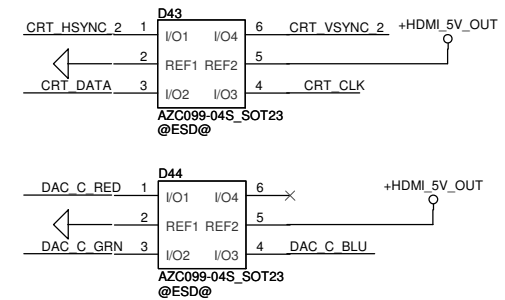
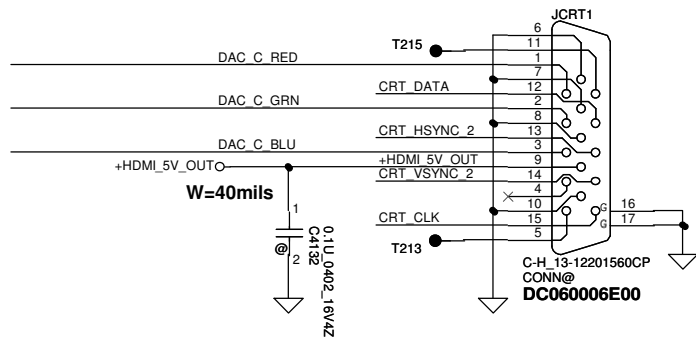
10/21 BOM change SM070003K00



HDMI Conn.



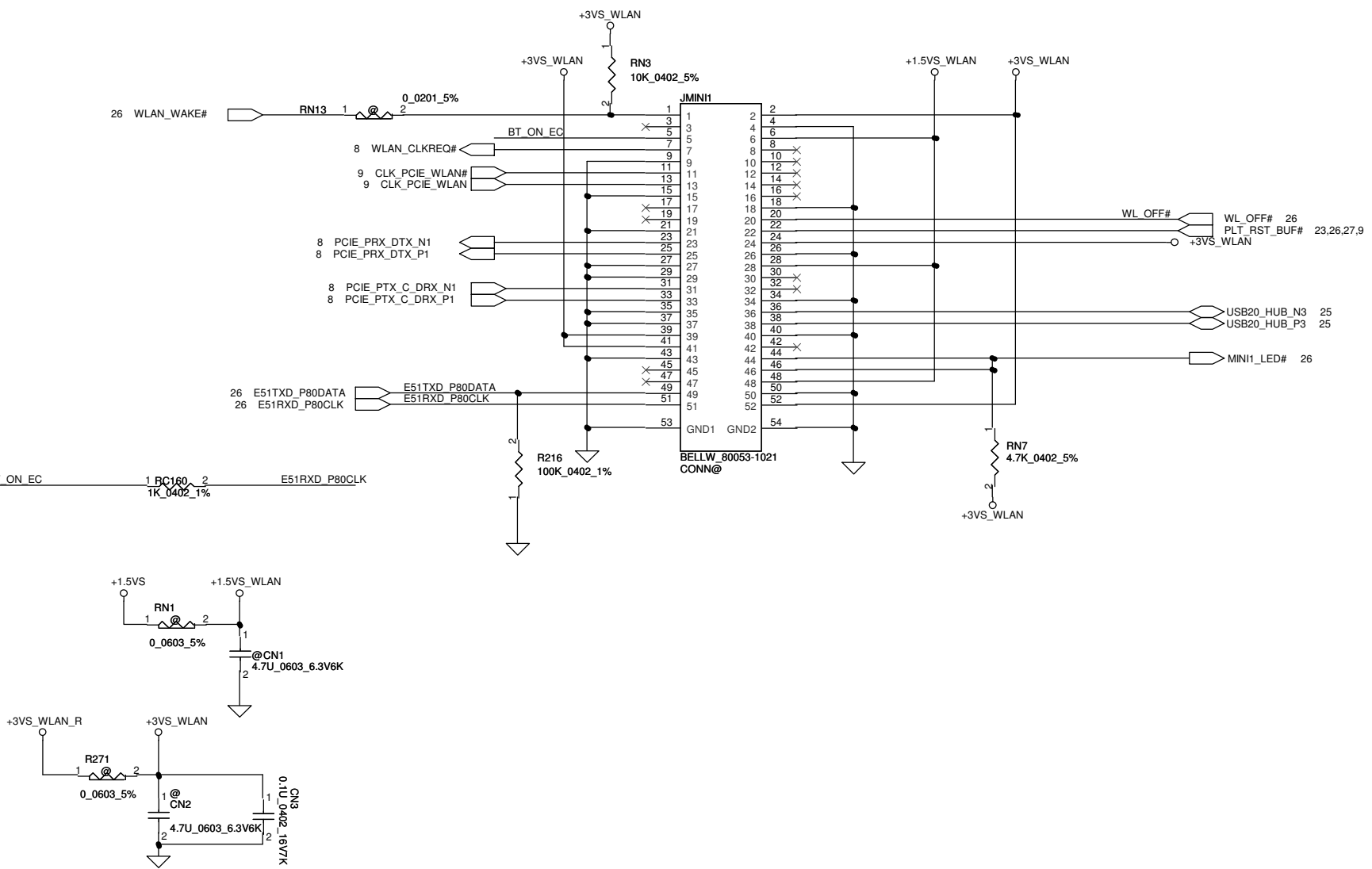
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	HDMI Conn/Level shift
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Issued Date				2013/02/26		Deciphered Date		2015/07/08		Title	
										CRT Connector	
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										LA-A994P	
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										0.1	
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										Sheet 19 of 43	

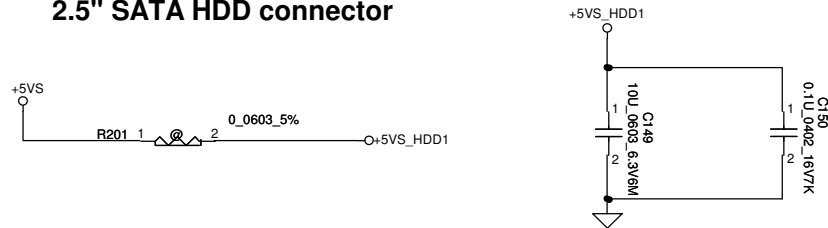
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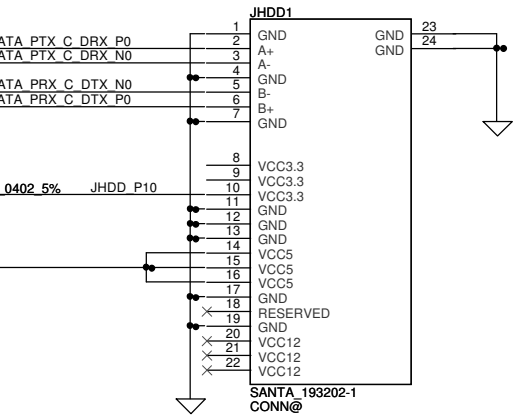
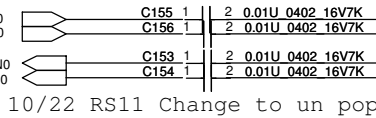


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				LA-A992P	Rev 0.1
Date: Friday, February 21, 2014				Sheet	21 of 43

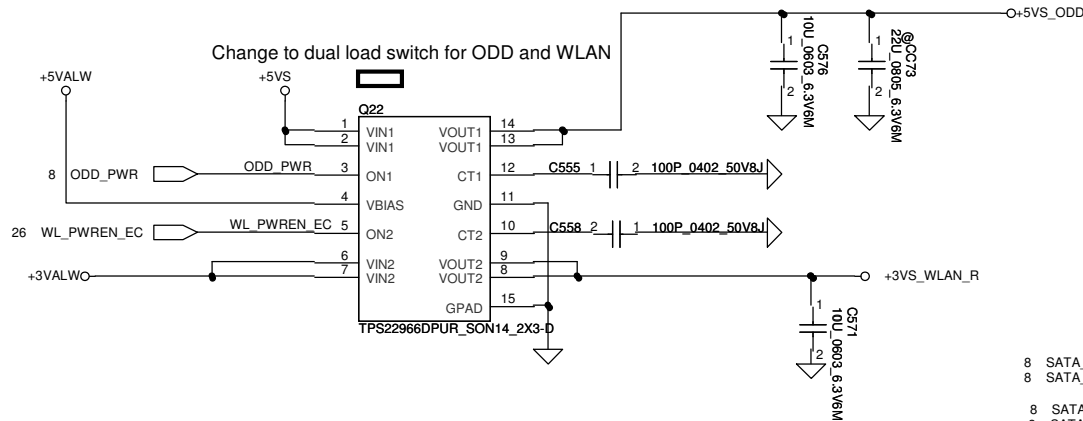
## 2.5" SATA HDD connector



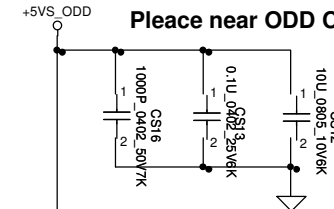
8 SATA\_PT\_X\_DRX\_P0  
8 SATA\_PT\_X\_DRX\_N0  
8 SATA\_PR\_X\_DTX\_N0  
8 SATA\_PR\_X\_DTX\_P0



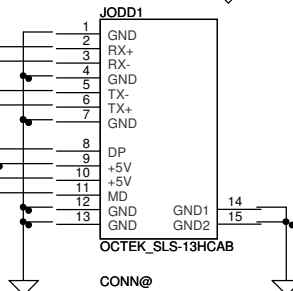
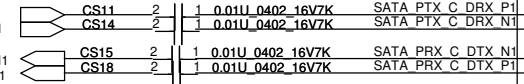
Change to dual load switch for ODD and WLAN



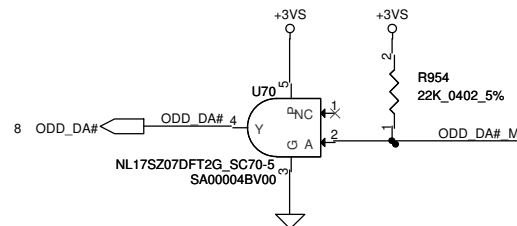
Place near ODD Connector



8 SATA\_PT\_X\_DRX\_P1  
8 SATA\_PT\_X\_DRX\_N1  
8 SATA\_PR\_X\_DTX\_N1  
8 SATA\_PR\_X\_DTX\_P1

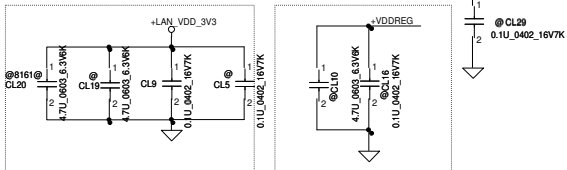
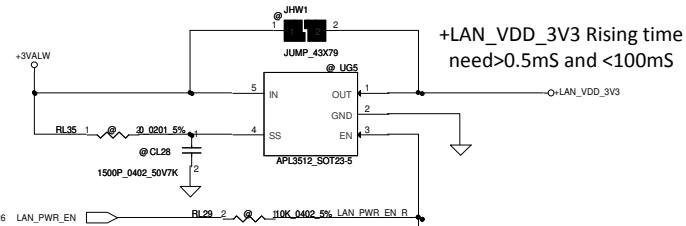


Place CS17 close to JODD



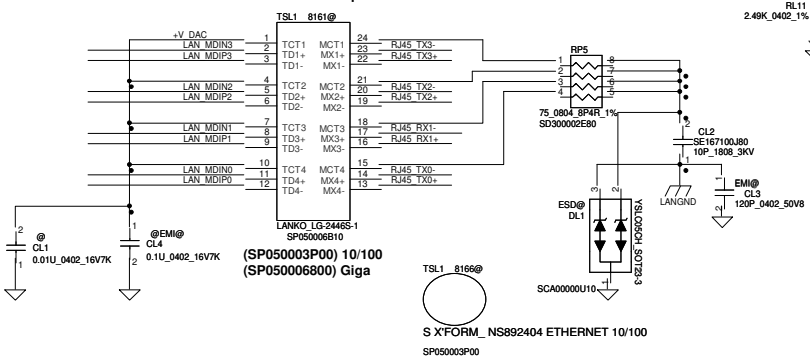
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				Date:	Friday, February 21, 2014
				Sheet	22 of 43

## JHW1 need to short



CL9 & CL5 close to UL1: Pin 11,32  
CL19 close to UL1: Pin 32  
CL20 close to UL1: Pin 11  
CL10 & CL16 close to UL1: Pin 23

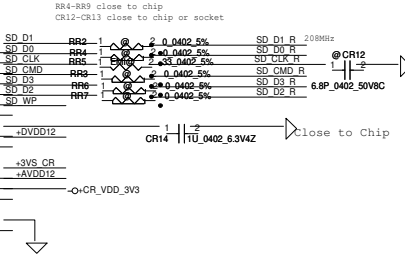
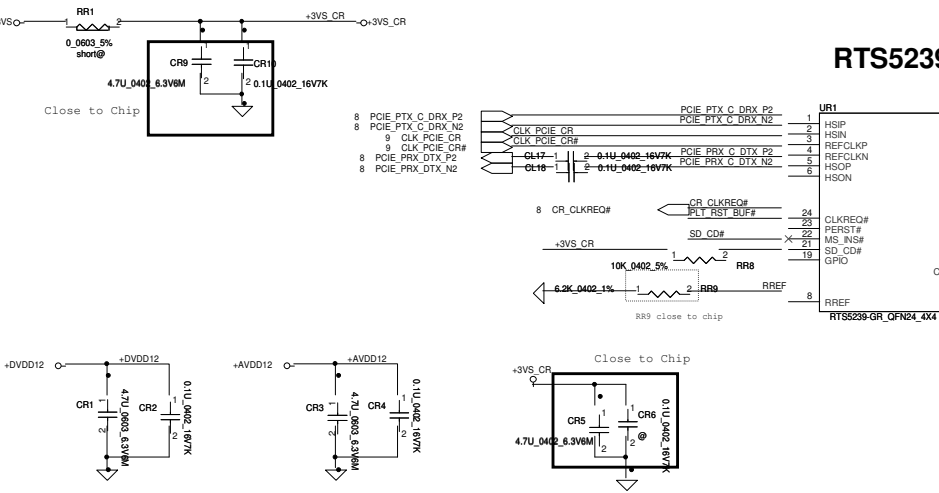
## SP050005L00 Footprint



(SP050003P00) 10/100  
(SP050006800) Giga

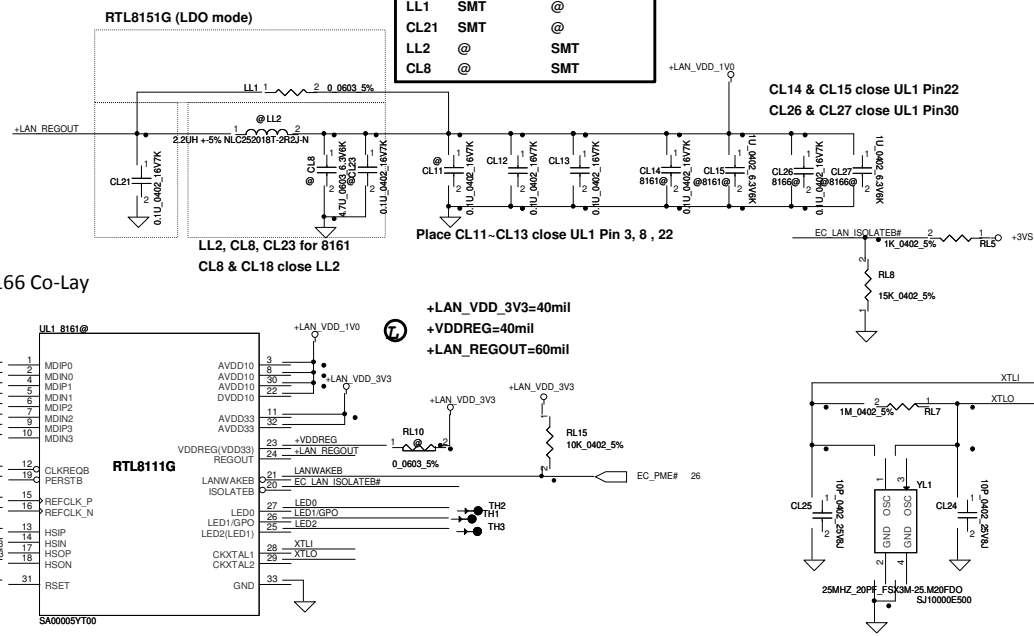
S X'FORM\_NS892404 ETHERNET 10/100  
SP050003P00

## RTS5239

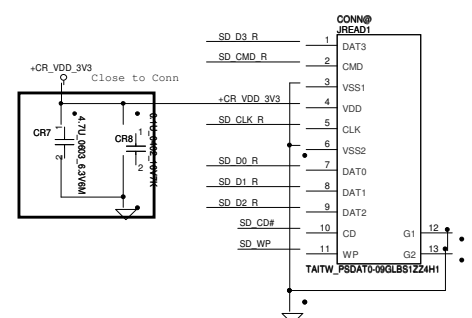


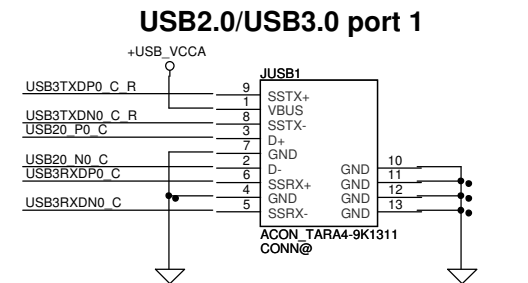
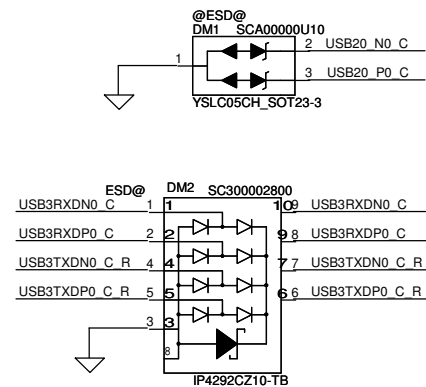
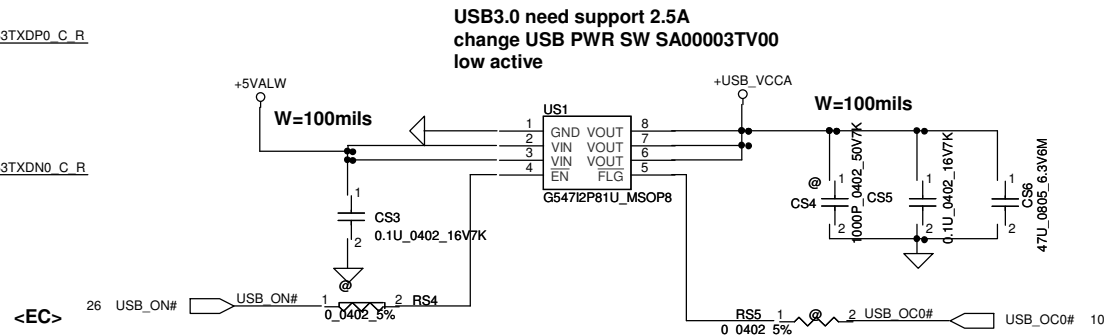
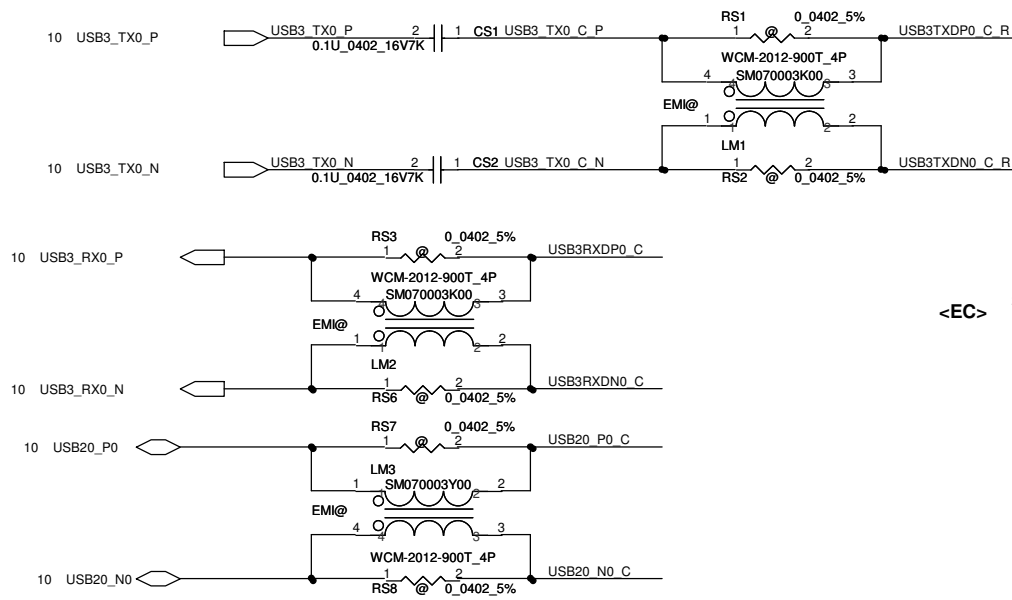
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LDO mode	Switching mode
LL1 SMT	@
CL21 SMT	@
LL2 @	SMT
CL8 @	SMT

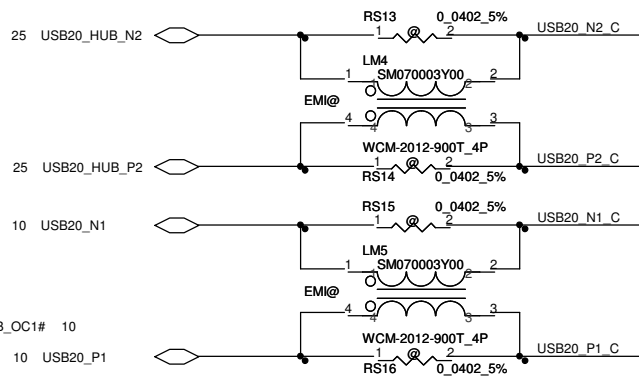
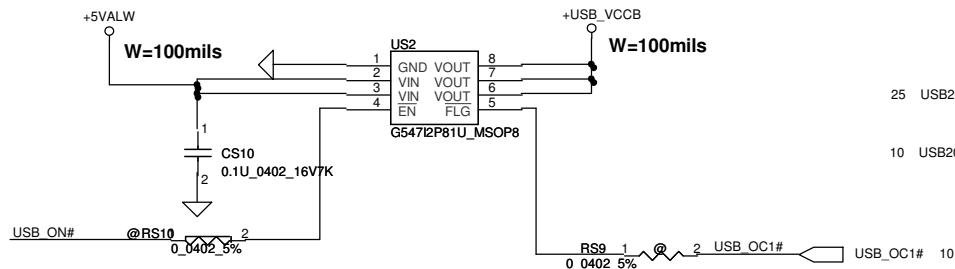


## Card Reader Connector

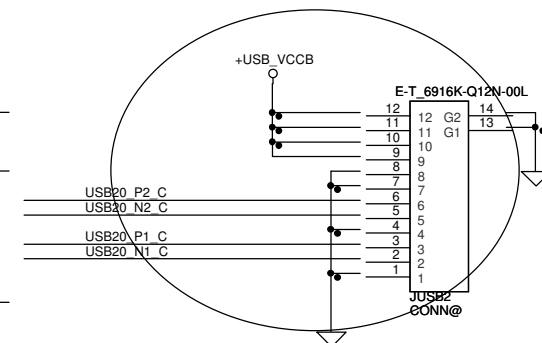




## USB2.0 port x 2



## 131109 Follow 15" Haswell LA-A992PR02



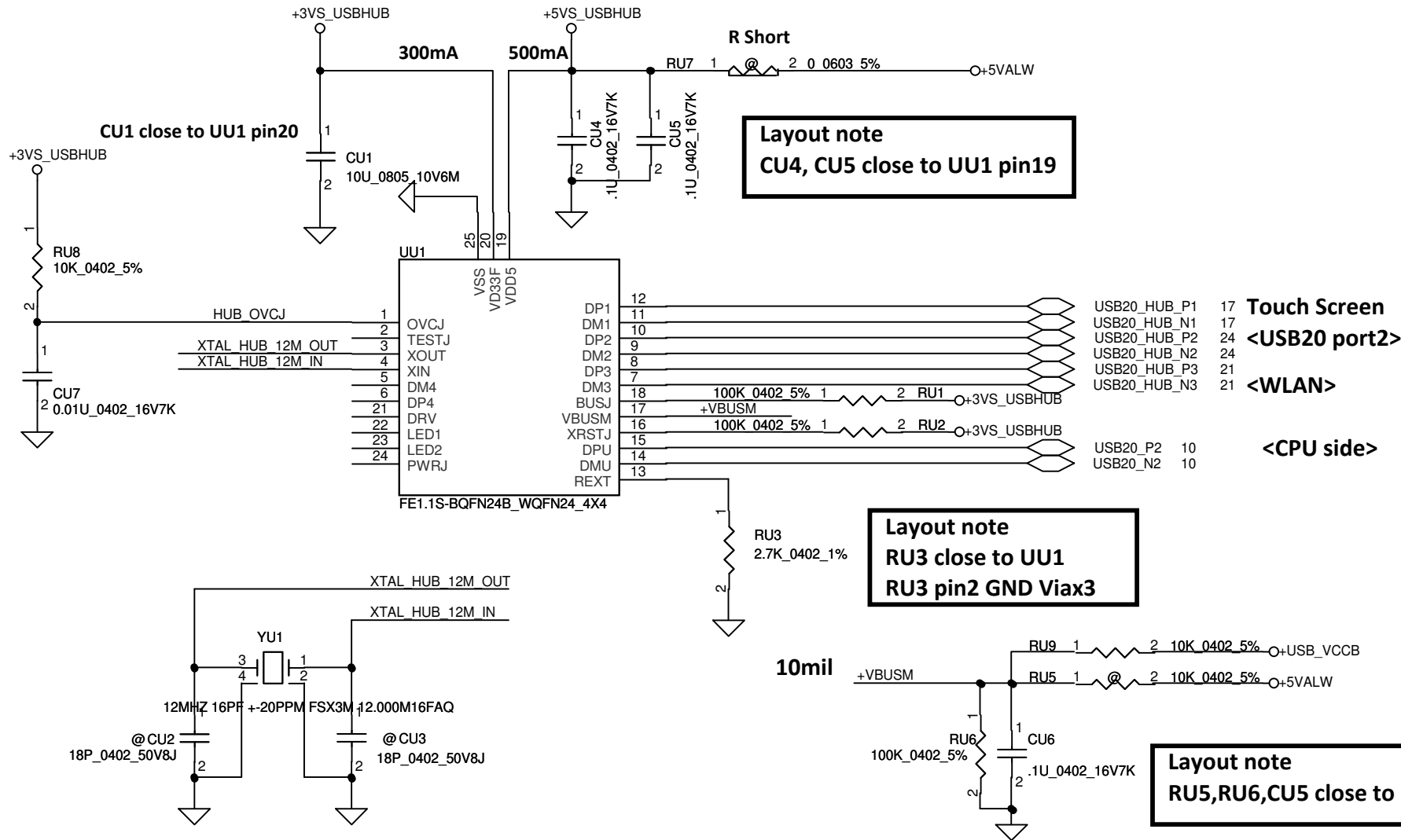
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	
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USB 3.0/2.0 conn

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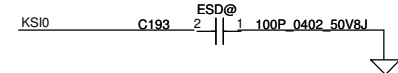
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2013/02/26	Deciphered Date	2015/07/08	Title
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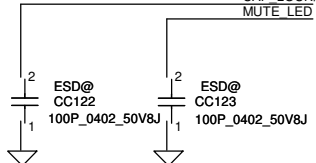
# TPM1.2

The diagram illustrates the connection of the TPM1.2 module to the U69 microcontroller. The U69 chip is shown with various pins connected to the TPM module (SLB 9656 TT 1.2). The connections are as follows:

- Power Supply:** +3VS, +3VSO, and +3VSD are connected to the U69 chip. The +3VSD is connected to the VSD pin of the TPM module.
- Signal Connections:**
  - LPC AD0, LPC AD1, LPC AD2, and LPC AD3 are connected to the LAD0, LAD1, LAD2, and LAD3 pins of the TPM module.
  - LPC CLK TPM is connected to the LCLK pin of the TPM module.
  - LPC FRAME# is connected to the LFRAME# pin of the TPM module.
  - PLT\_RST\_BUF# is connected to the LRESET# pin of the TPM module.
  - EC\_SERIRQ is connected to the SERIRQ pin of the TPM module.
  - LCLK is connected to the LCLK pin of the TPM module.
  - LFRAME# is connected to the LFRAME# pin of the TPM module.
  - LRESET# is connected to the LRESET# pin of the TPM module.
  - SERIRQ is connected to the SERIRQ pin of the TPM module.
  - CLKRUN# is connected to the CLKRUN# pin of the TPM module.
  - PP is connected to the PP pin of the TPM module.
  - GPIO2 is connected to the GPIO2 pin of the TPM module.
  - GPIO is connected to the GPIO pin of the TPM module.
- TPM Module Connections:** The TPM module (SLB 9656 TT 1.2) has pins for LCPD#, TESTB1/BADD, TEST1, XTALO, XTALI, GPIO2, GPIO, NC, and GND. The XTALO and XTALI pins are connected to the T45 PAD and T46 PAD respectively. The GPIO2 and GPIO pins are connected to the T45 PAD and T46 PAD respectively. The NC pins are connected to the T45 PAD and T46 PAD respectively. The GND pins are connected to the T45 PAD and T46 PAD respectively.

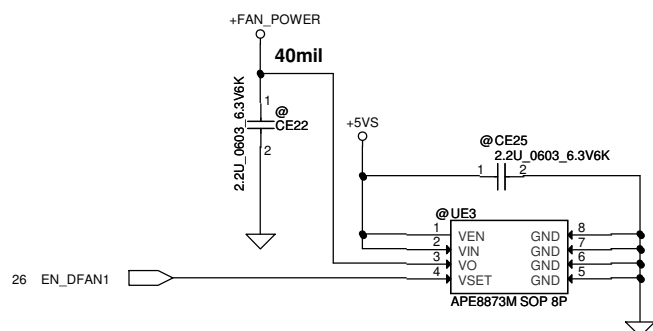
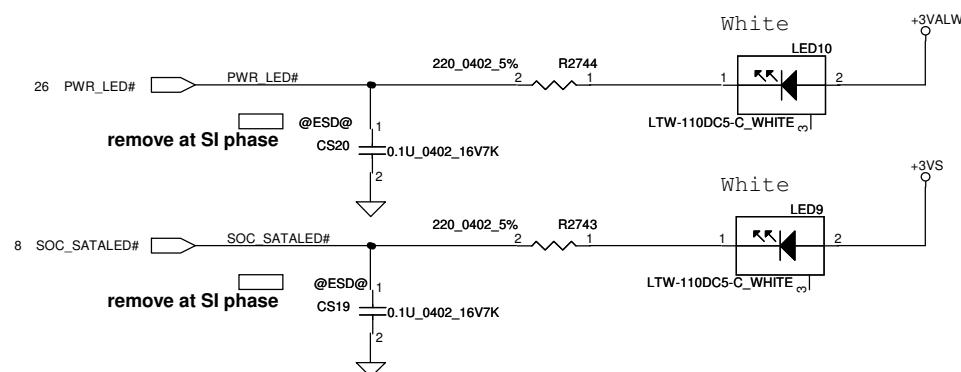
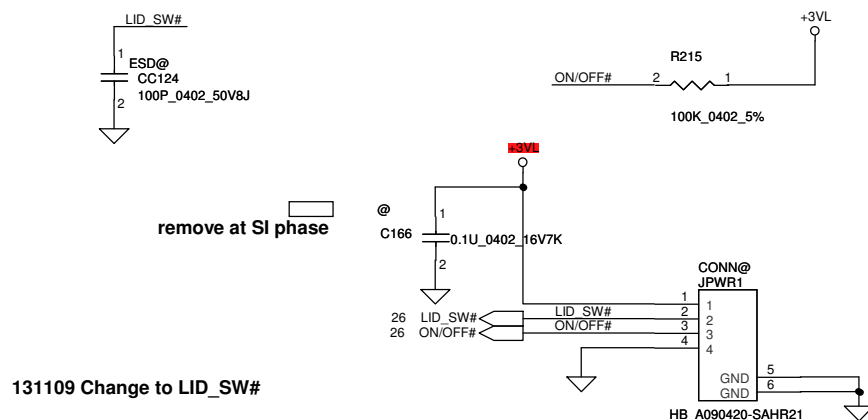


10/24 ESD@ Change @ESD@

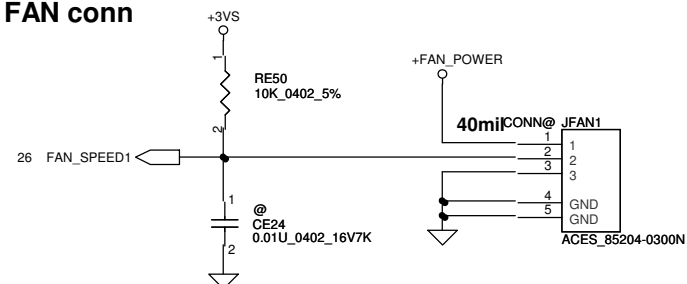


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# Power Button Connector

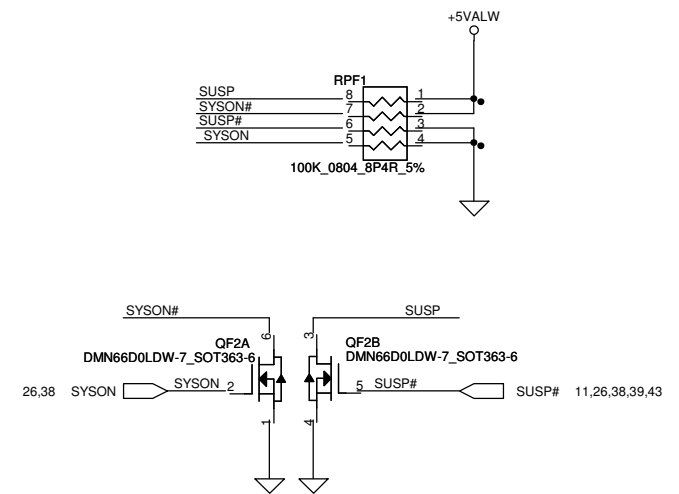
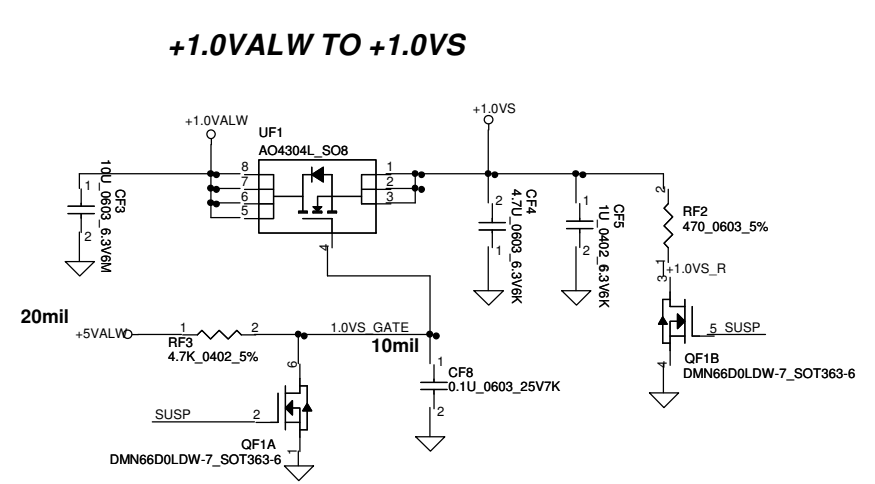


## FAN conn



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				0.1
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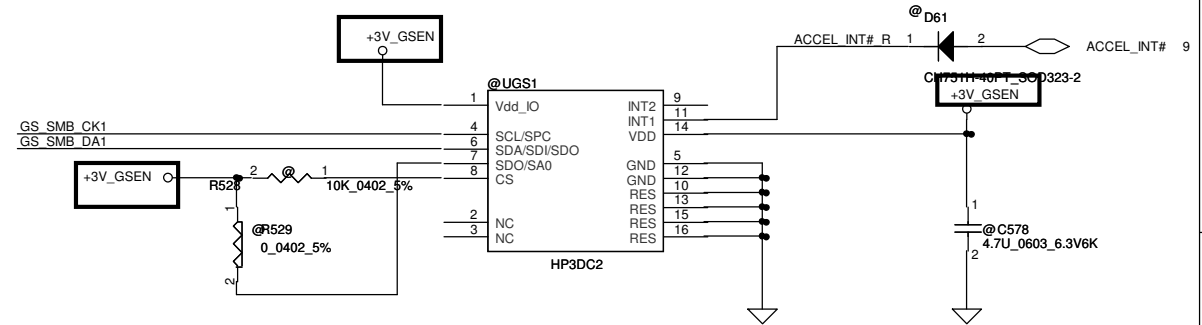
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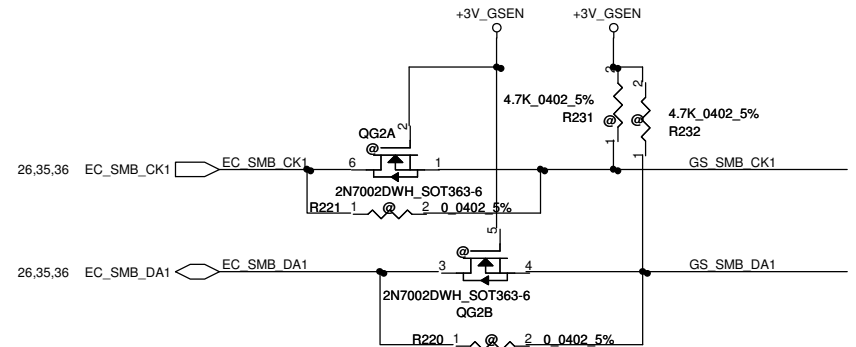
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10/21 +3VALW Change +3VL

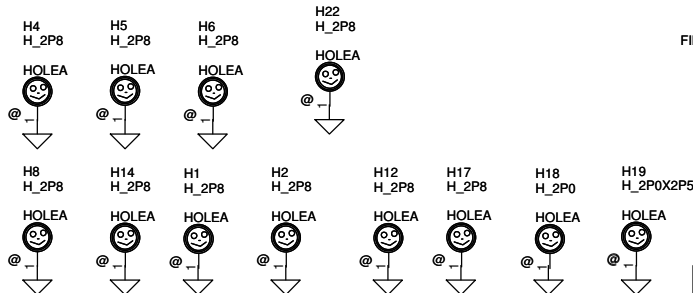
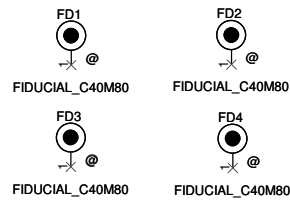
# ACCELEROMETER



Ⓛ Must be placed in the center of the system.

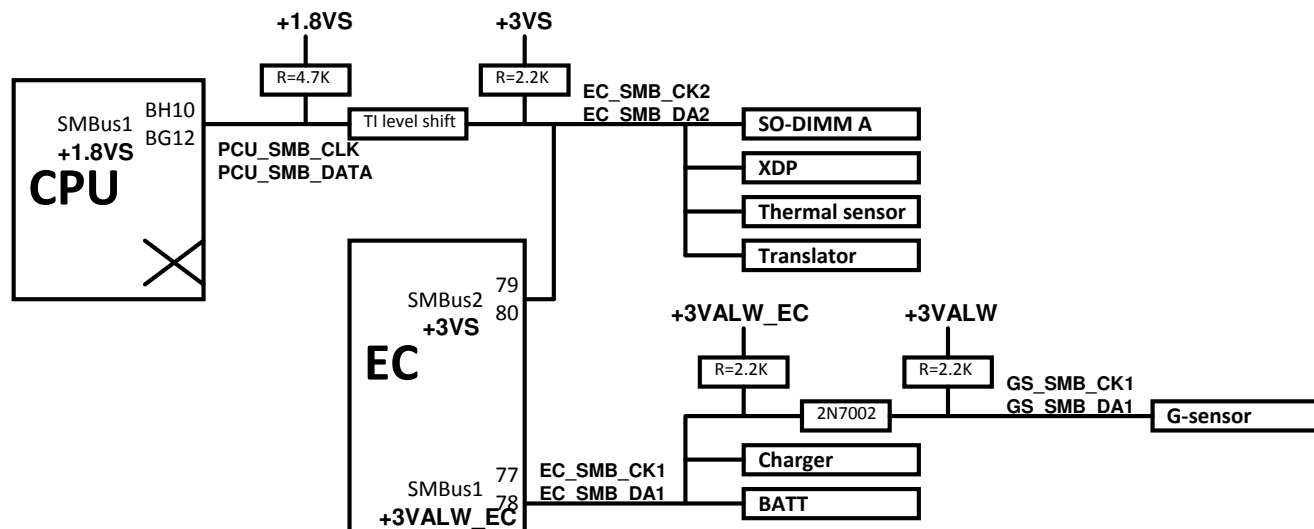


Reserve MOS for power leakage



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## <SMBus Routing>



<USB2.0/3.0 port>

USB2.0	USB3.0	Function	Note
0	X	Left port (USB2.0)	
1	0	Right port-1 (USB2.0/3.0)	
2	X	Right port-2 (USB2.0)	
3	X	WLAN	USB2.0x4 Hub
4	X	Touch screen	USB2.0x4 Hub
5	X	Camera	USB2.0x4 Hub
6	X	NC	USB2.0x4 Hub

<PCI-E port>

PCI-E	Function	Note
0	LAN	
1	WLAN	
2	Card reader	
3	NC	

<SATA port>

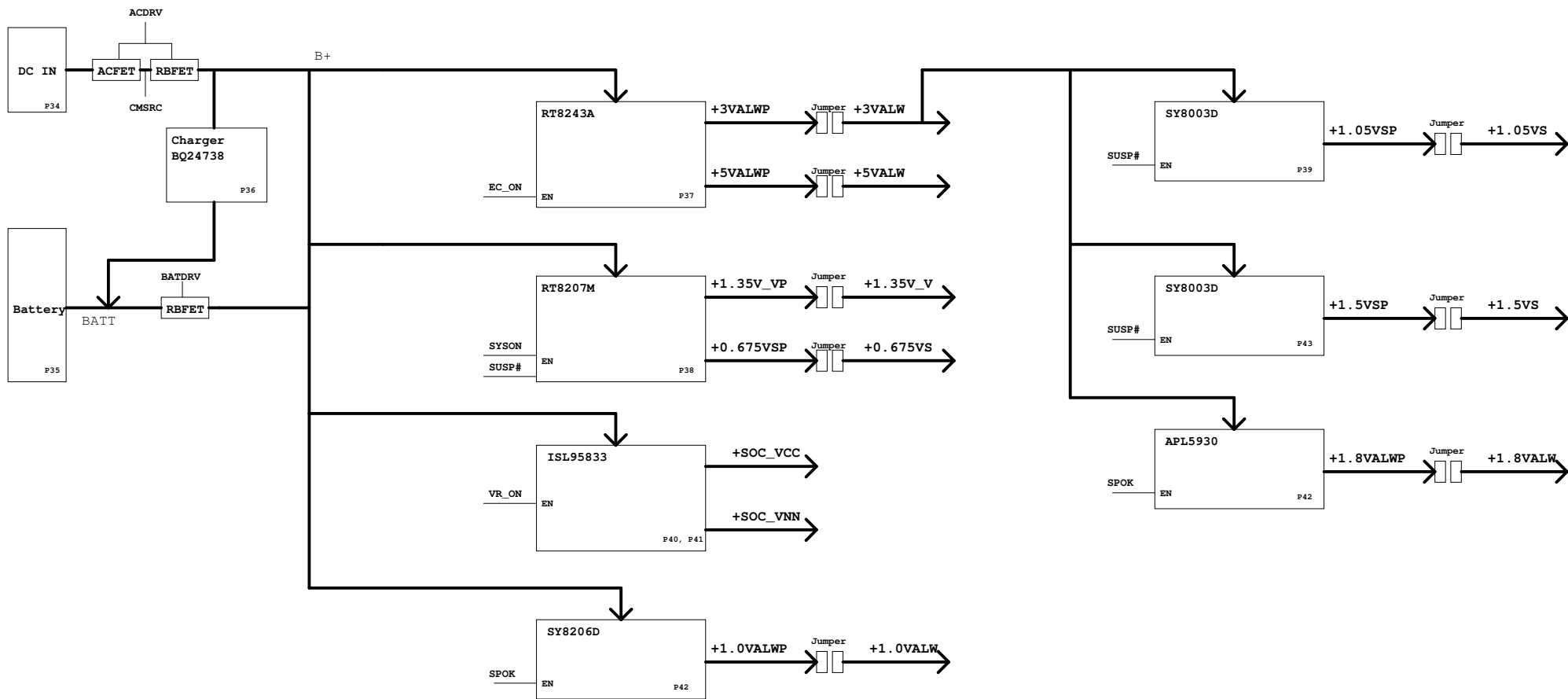
PCI-E	Function	Note
0	HDD	
1	NC	

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				Size	Document Number	Rev
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Date:				Sheet	31	of 43

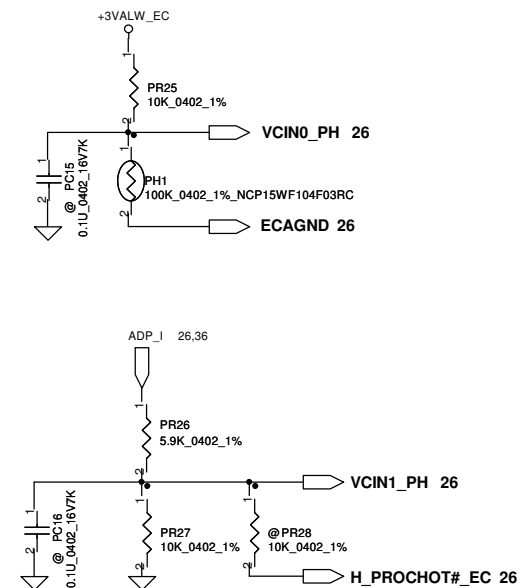
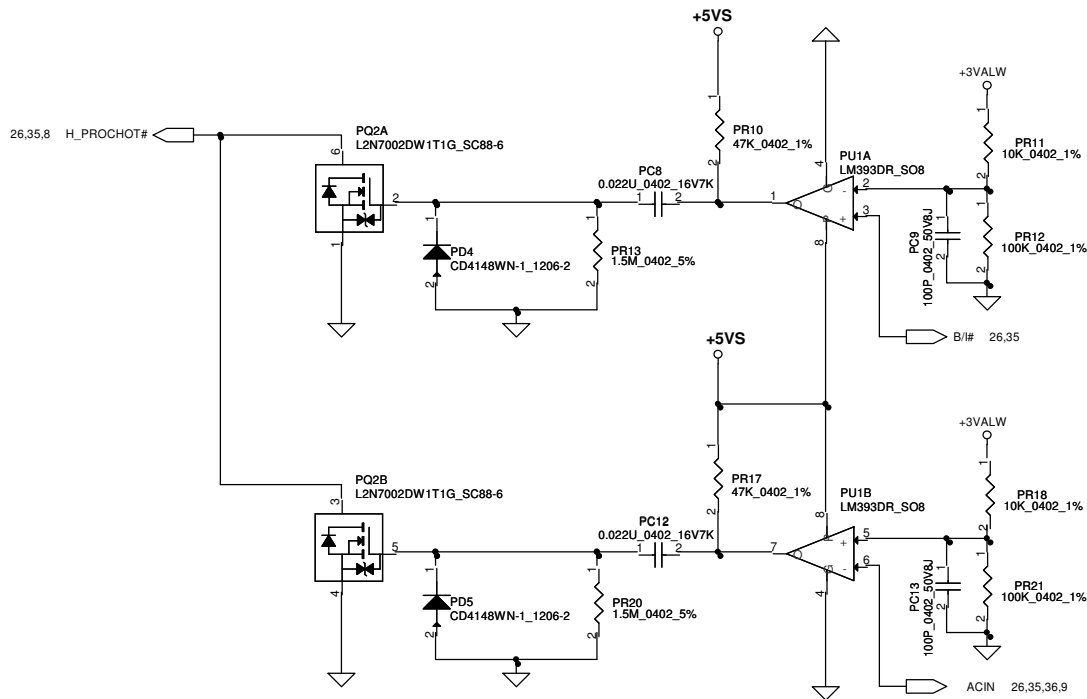
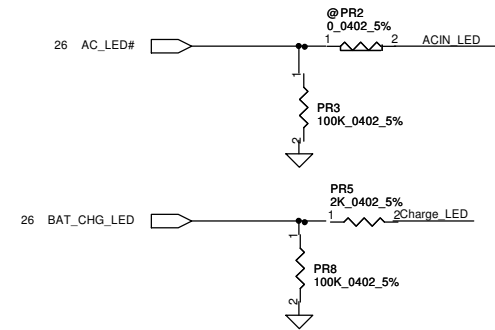
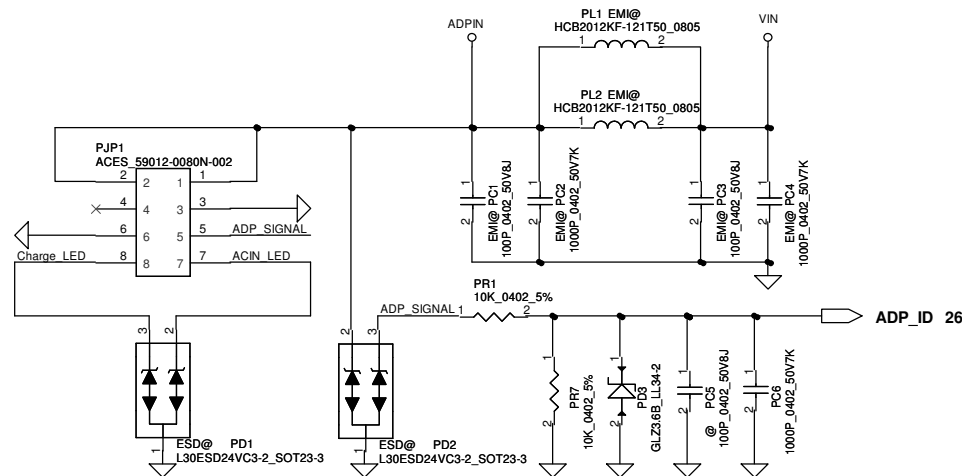
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29		131107		1.Change PN of RPF1 from SD302100380 to SD309100380		
2	28		131109		1.Change Control pin of LID from NEW_LID_SW(R218) to LID_SW#(R219)		
3	24		131109		1.Follow 14" Haswell LA-A993PRO2's USB2 Conn.		
4	16		131111		1.Update UT3 footprint follow Haswell platform		
5	22		131111		1.Delete R954 ,Q84 for ODD_DA# 2.unpop RS11		
6	18		131111		1.Change PN of LM13,LM14,LM15 & LM16 from SM070001V00 to SM070003K00		
7	30		131111		1.Change Power Rail of G sensor from +3VALW to +3VL & unpop QG2		
8	30		131111		1.pop DM5		
9	26		131111		1.change Board ID to SI phase		
10	16		131111		1.add PD 100K RT15K for power sequence		

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				HW PIR	
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				Document Number	0.1
Date				Friday, February 21, 2014	Sheet 32 of 43

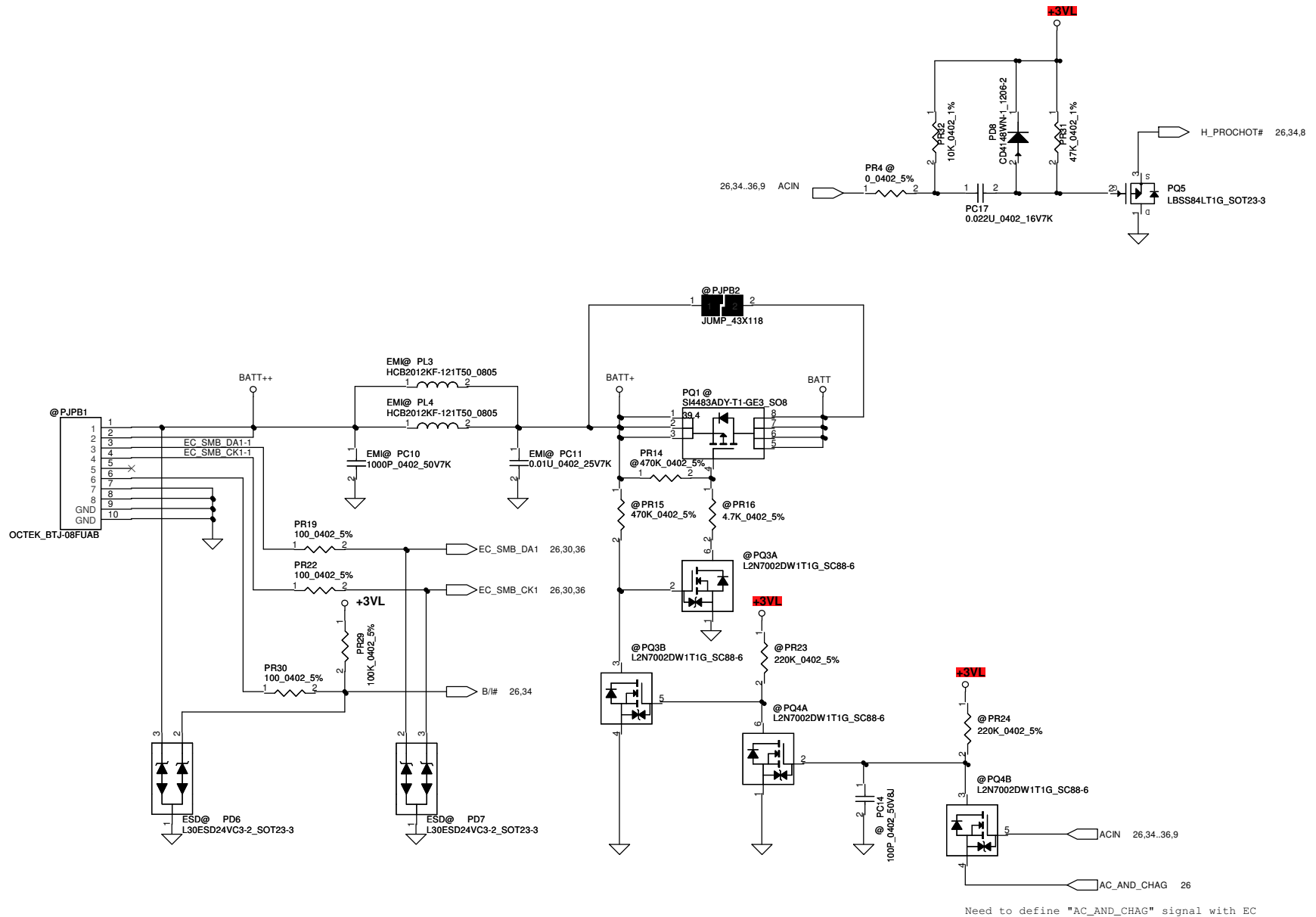




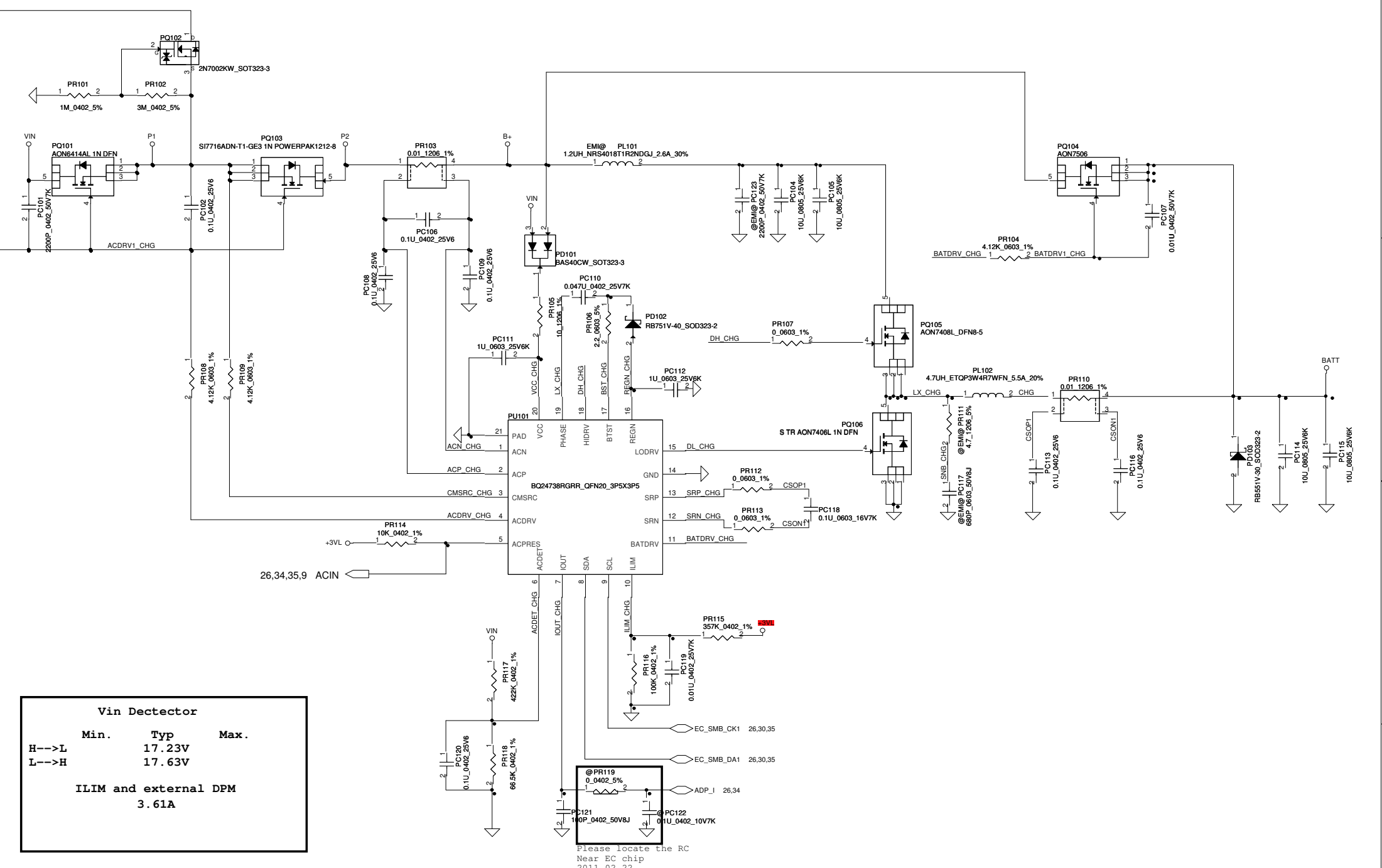
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/20	Deciphered Date	2016/08/31	Title	Power Block Diagram
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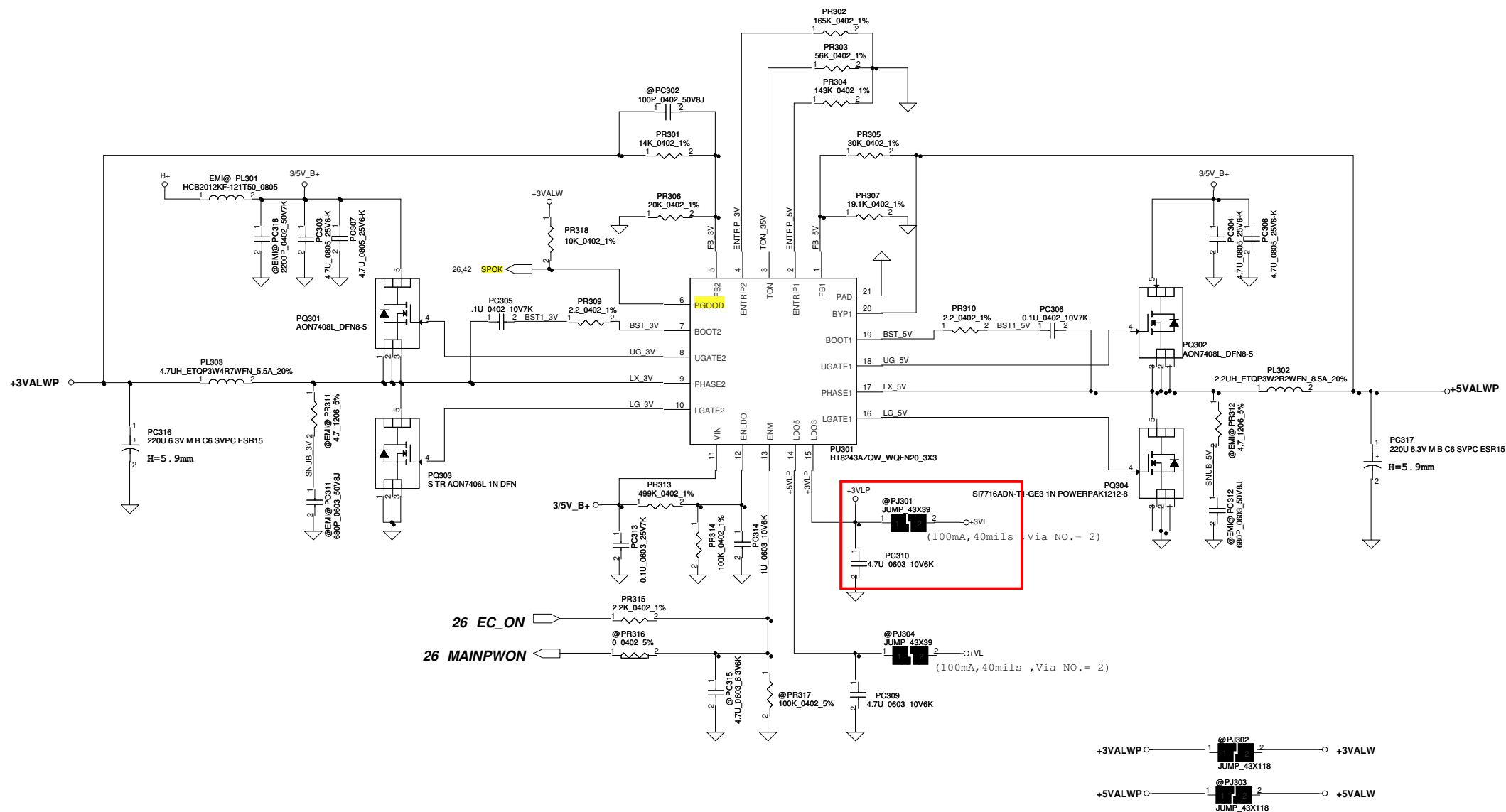
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Vin Detector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM  
3.61A



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**Design Note**  
 This circuit is for ULC 1+1 7.5W.  
 CPU: Icc=12A  
 Loadline: -5.9 m V/A  
 GFX(GT2): Icc=14A  
 Loadline: -5.9 m V/A

For VR\_HOT#, already  
 pull high at power side.

PR18 and PR30  
 27.4K ohm for 100 degree  
 61.9K ohm for 110 degree

**Layout Note**  
 SVID routing  
 1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.  
 2. SVID spacing requirement is 18mils(0.475mm)/VSSSENSE  
 3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).  
 4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.  
 5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.  
 6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$   
 If  $C_n$  is correctly selected, when the load current has a square change, the output voltage also has a square response.

**Layout Note**  
 Reduce Acoustic Noise  
 1. The AL bulk capacitor of B+ should be very close to CPU\_CORE MOSFET.  
 2. Input ceramic caps must place on symmetry same location on top side and bottom side.

MDV1525 Vds=30V  
 Rds(on)=11.5-14m ohm@Vgs=4.5V

OCP setting=-20A  
 MDV1525 Vds=30V  
 Rds(on)=2.7-3.3m ohm@Vgs=4.5V

VDD source use +5VS and PG00D source use +3VS  
 Please confirm power on and down sequence,  
 make sure VGATE after CPU\_CORE on.

MDV1525 Vds=30V  
 Rds(on)=11.5-14m ohm@Vgs=4.5V

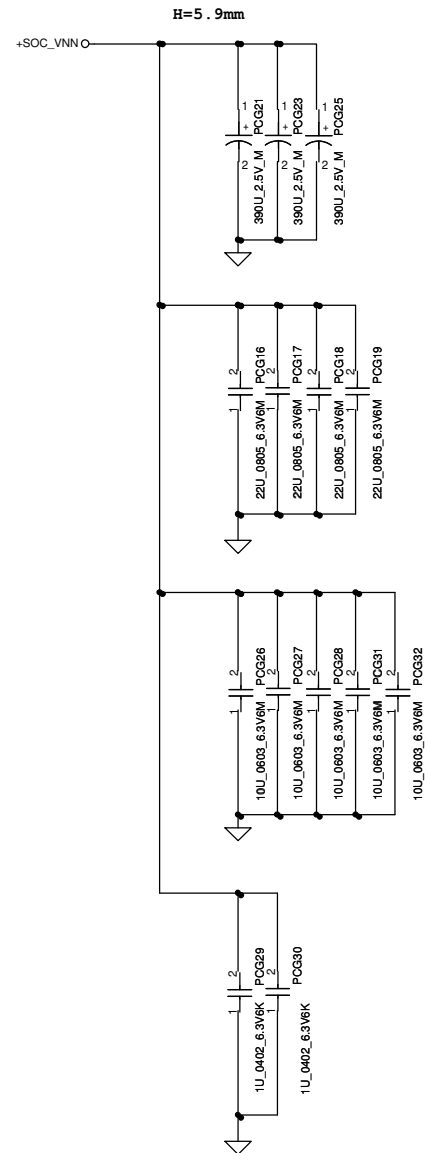
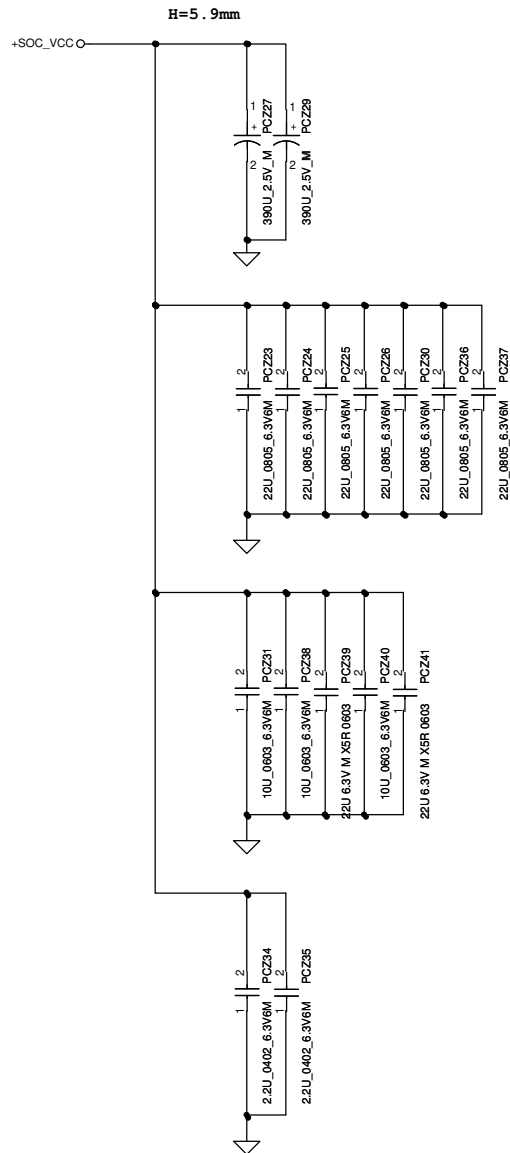
MDU1511 Vds=30V  
 Rds(on)=2.7-3.3m ohm@Vgs=4.5V

Close CPU choke

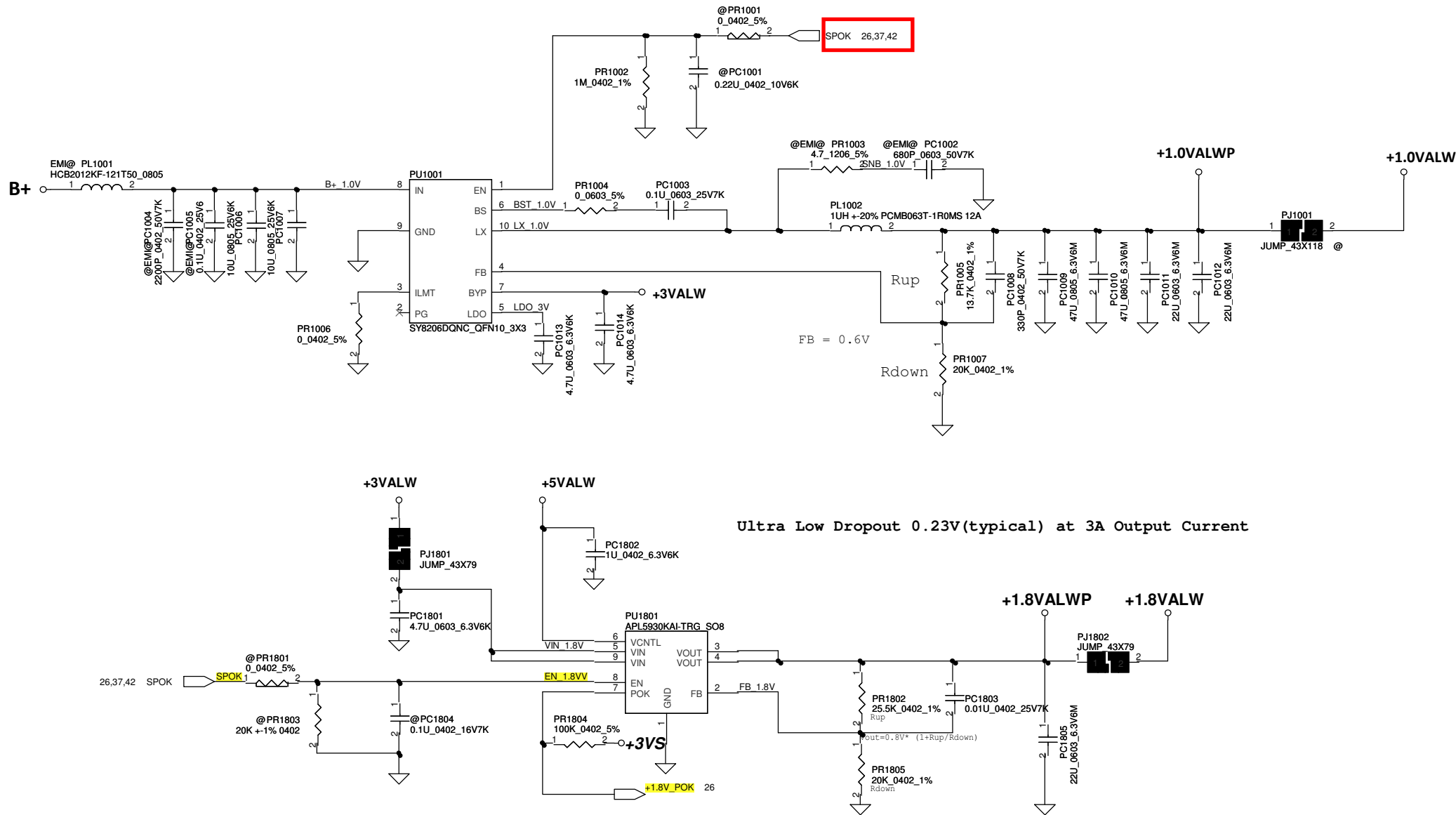
OCP setting=-18A

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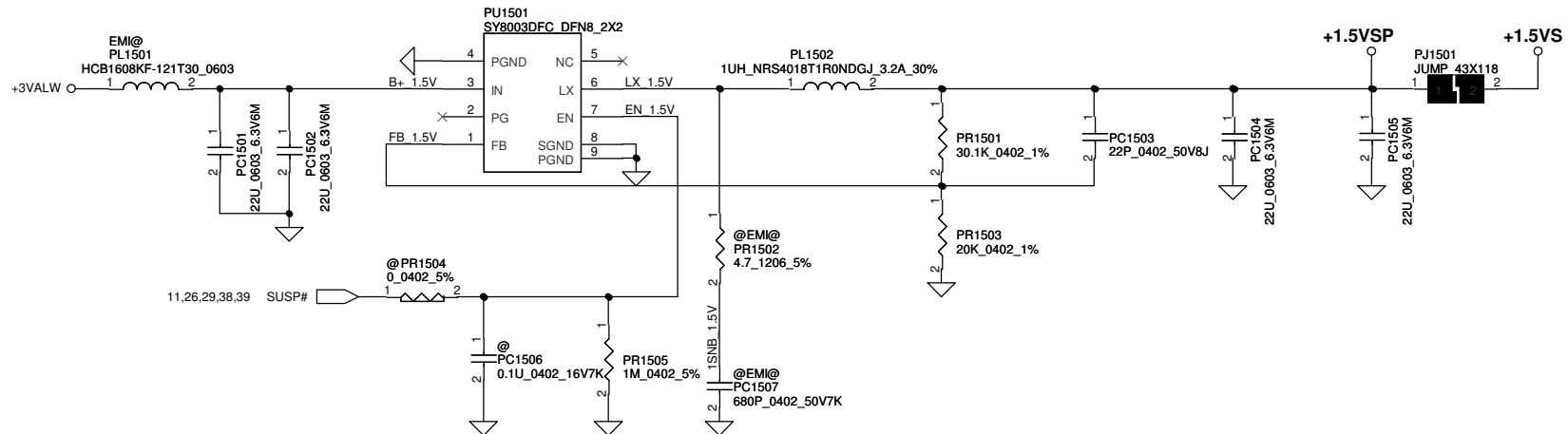




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